
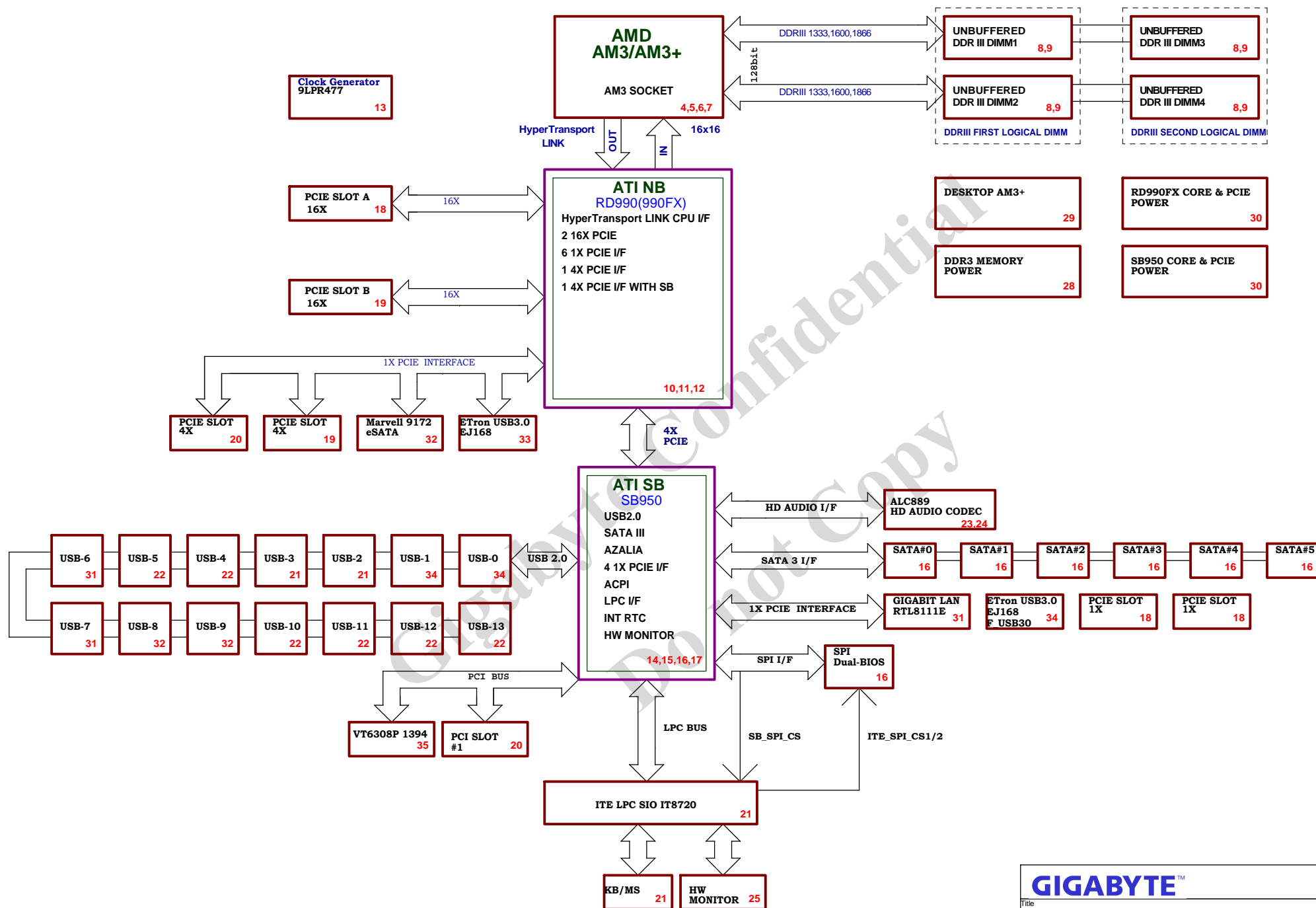


www.xinxunwei.com 400-800-9990

PAGE	TITLE
------	-------

			
Title <span style="float: right; font-weight: bold; font-size: 1.2em;">COVER SHEET</span>			
Size	Document Number	GA-990FXA-UD3	Rev <b>1.11</b>
Date:	Monday, May 07, 2012	Sheet 1 of 35	

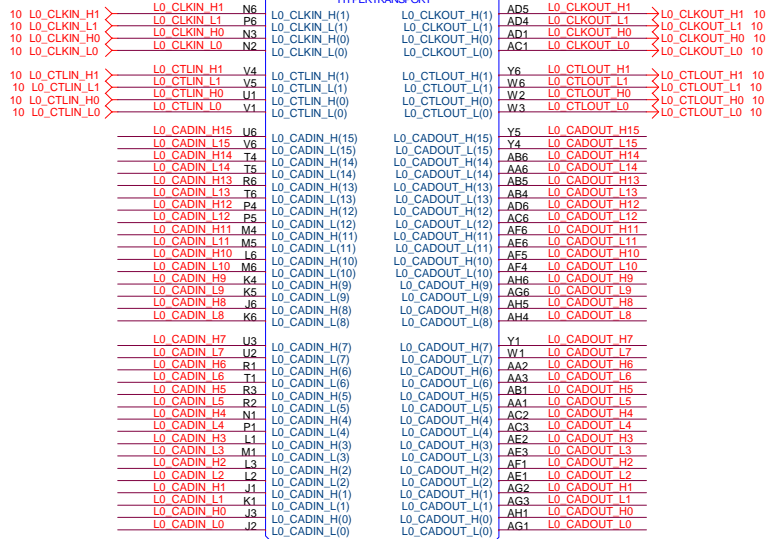




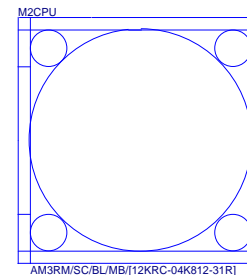
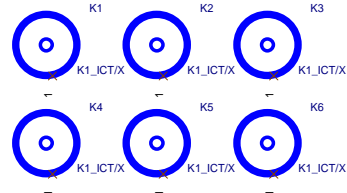
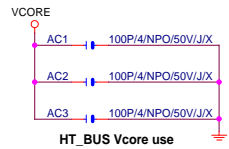
L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] 10  
 L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] 10  
 L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] 10  
 L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] 10

M2CPUA

HYPERTRANSPORT

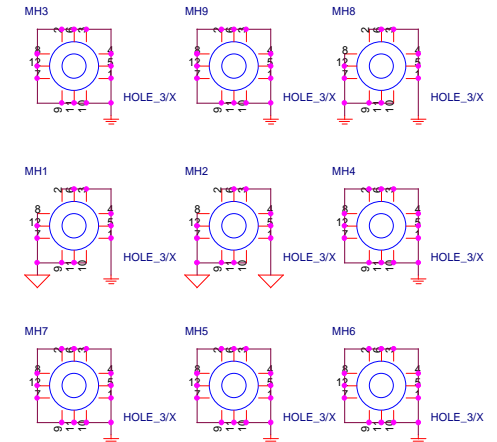


CPU-SK/941AM3/S/GF/[10SC1-A01942-01R\_10SC1-A01942-02R]

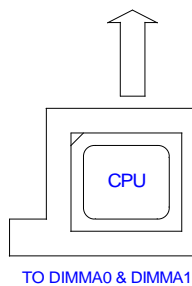
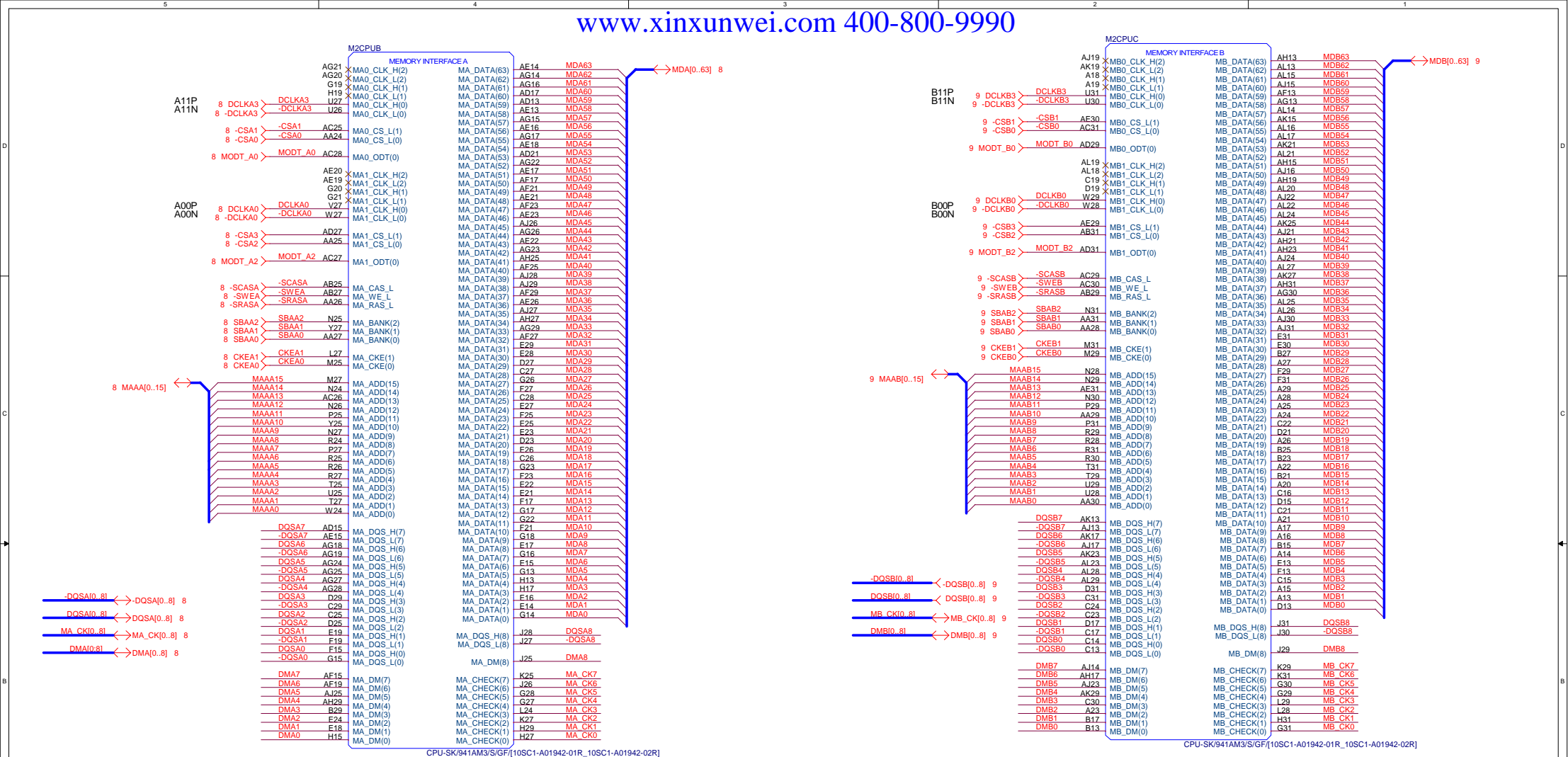


CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

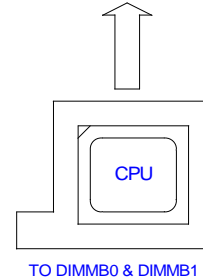
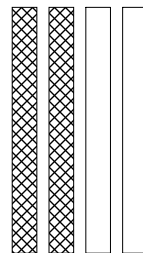
VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B



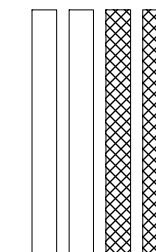
<b>GIGABYTE™</b>		
Title <b>COVER SHEET</b>		
Size	Document Number	Rev
Custm	<b>GA-990FXA-UD3</b>	<b>1.11</b>
Date:	Monday, May 07, 2012	Sheet 4 of 35



MEM CHA



MEM CHB



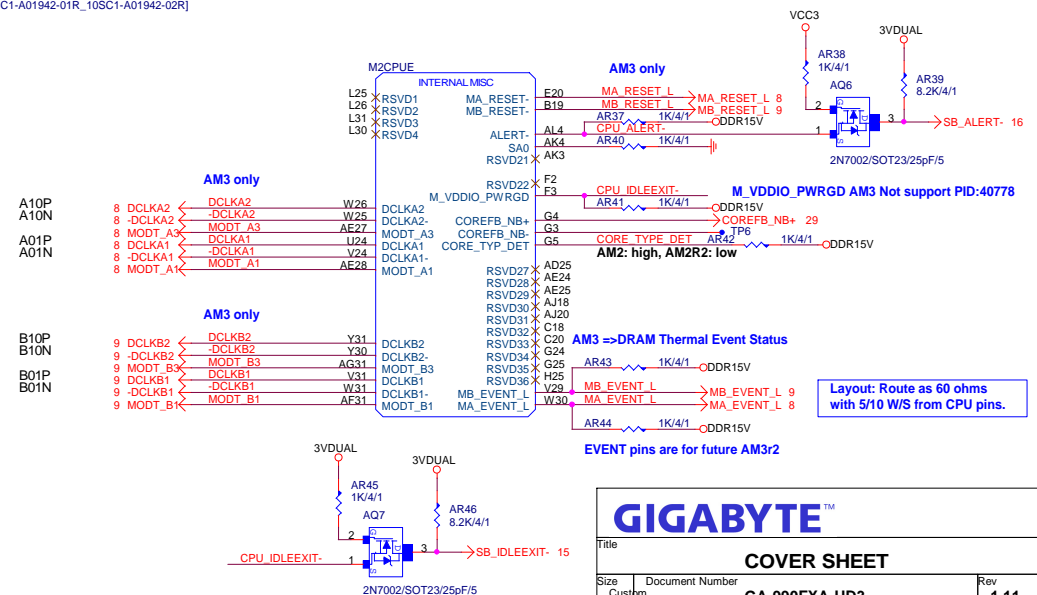
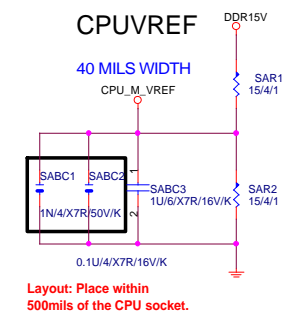
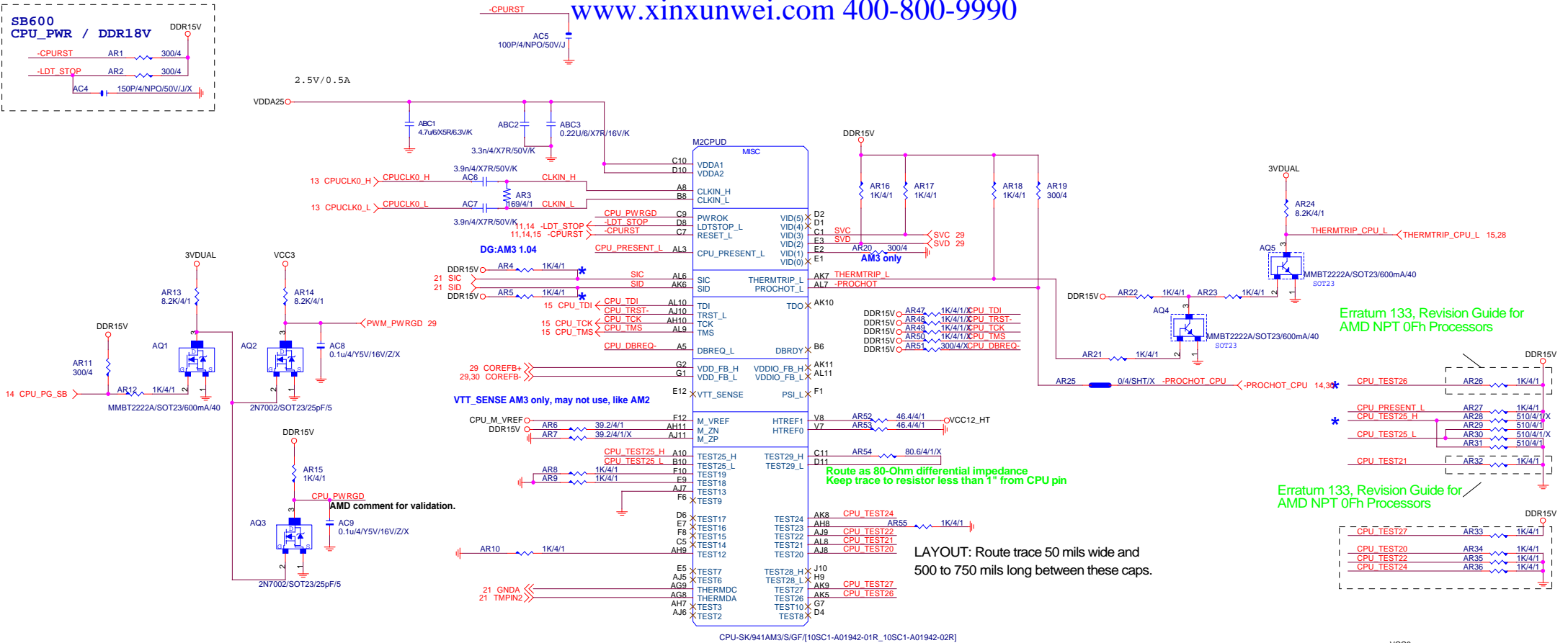
**GIGABYTE™**

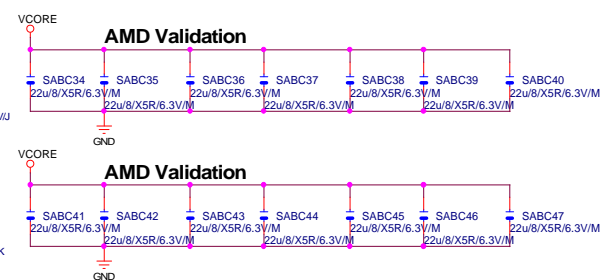
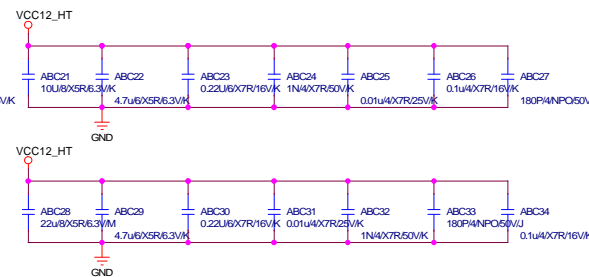
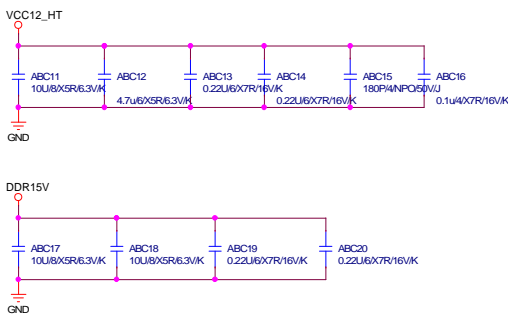
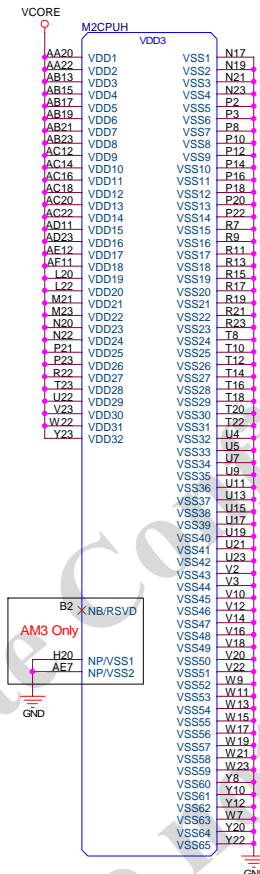
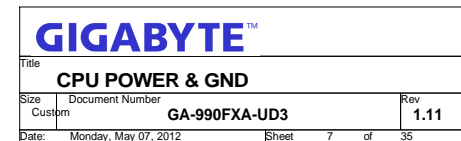
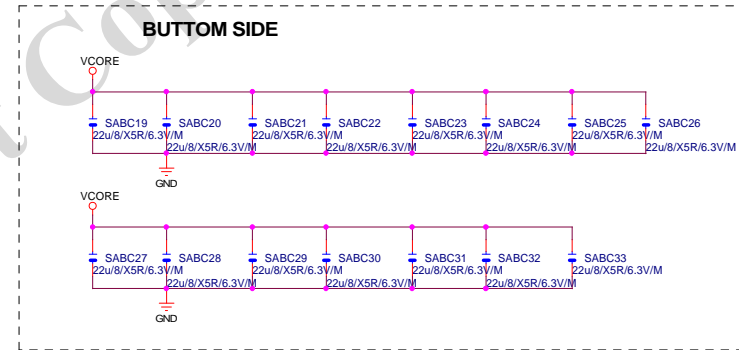
**COVER SHEET**

Title: GA-990FXA-UD3

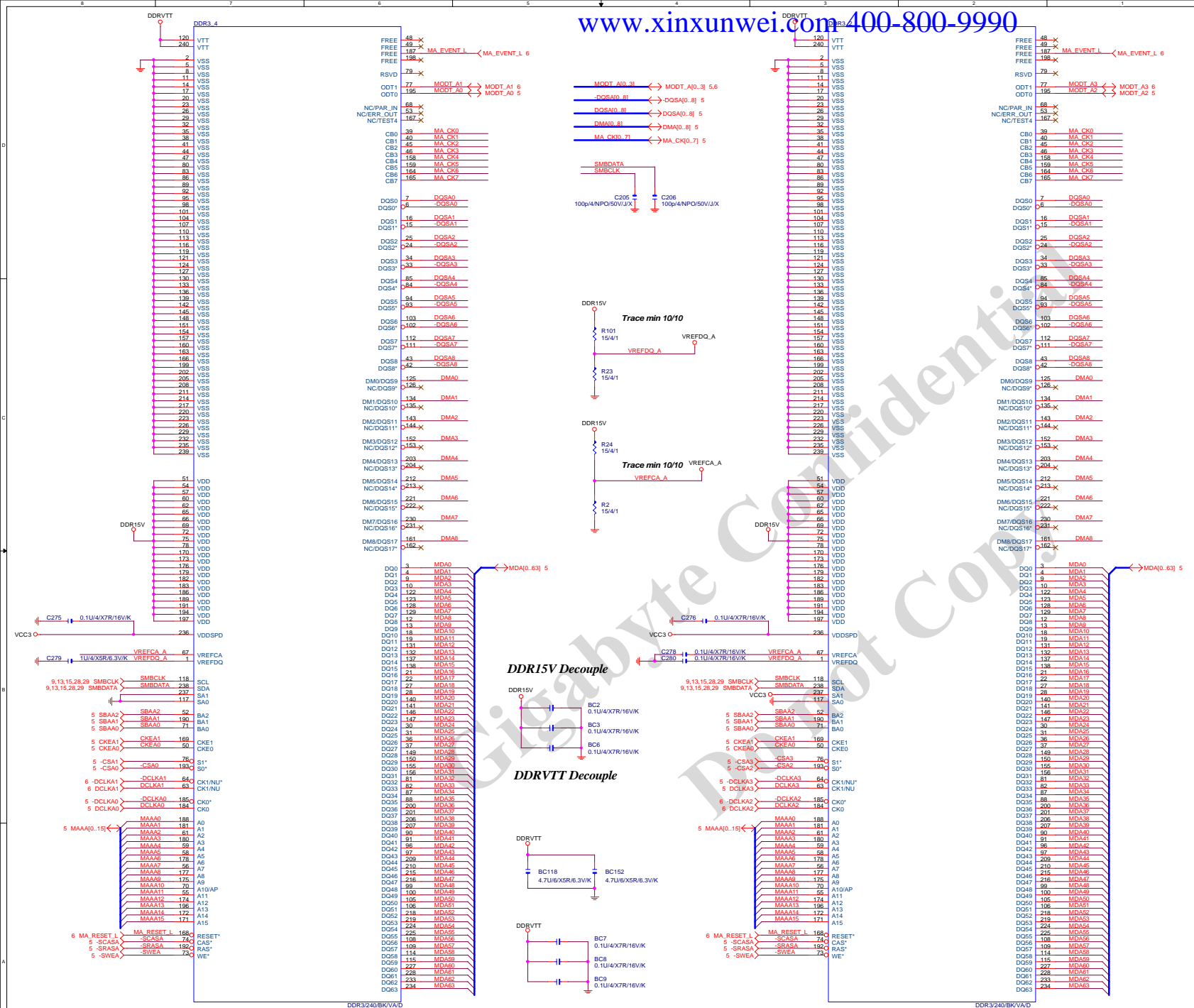
Size: Custom Document Number: GA-990FXA-UD3 Rev: 1.11

Date: Monday, May 07, 2012 Sheet: 5 of 35

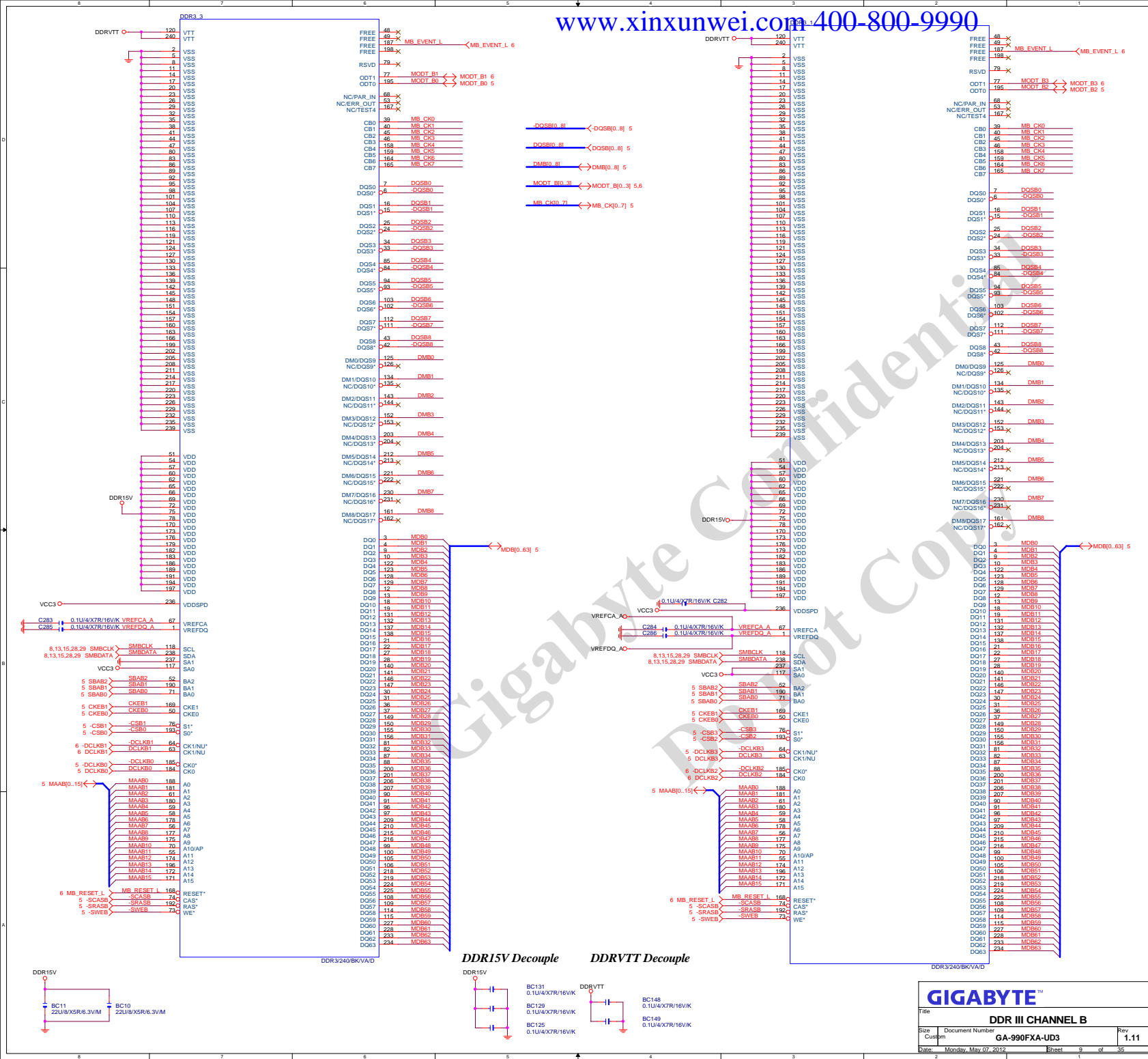












U3A

## PART 1/5

L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15
L0_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10
L0_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	F24	L0_CADIN_H9
L0_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8
L0_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	N27	L0_CADIN_L7
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M27	L0_CADIN_H6
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	M28	L0_CADIN_L6
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L26	L0_CADIN_H5
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	L27	L0_CADIN_L5
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K27	L0_CADIN_H4
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	K28	L0_CADIN_L4
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	J28	L0_CADIN_L3
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	G26	L0_CADIN_H2
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G27	L0_CADIN_L2
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	F27	L0_CADIN_H1
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F28	L0_CADIN_L1
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	E28	L0_CADIN_H0
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E27	L0_CADIN_L0
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N		

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
4 L0_CTOUT_H1	L0_CTOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
4 L0_CTOUT_L1	L0_CTOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
4 L0_CTOUT_H0	L0_CTOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P27	L0_CTLIN_H0	L0_CTLIN_H0	4
4 L0_CTOUT_L0	L0_CTOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P28	L0_CTLIN_L0	L0_CTLIN_L0	4

SNR0	1.21K/4/1	HT_RXCALN	D25	HT_RXCALP	NR1	1.21K/4/1
		HT_RXCALN	D24	HT_RXCALN		

L0_CADIN_H10_15]	L0_CADIN_H10_15]	4
L0_CADIN_L10_15]	L0_CADIN_L10_15]	4

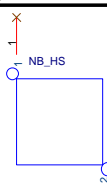
4 L0_CADOUT_H10_15]	L0_CADOUT_H10_15]	
---------------------	-------------------	--

4 L0_CADOUT_L10_15]	L0_CADOUT_L10_15]	
---------------------	-------------------	--

EXP_A_RXP10_15]	EXP_A_RXP10_15]	18
EXP_A_RXN10_15]	EXP_A_RXN10_15]	18
EXP_A_TXP10_15]	EXP_A_TXP10_15]	18
EXP_A_TXN10_15]	EXP_A_TXN10_15]	18

EXP_B_TXP10_15]	EXP_B_TXP10_15]	19
EXP_B_TXN10_15]	EXP_B_TXN10_15]	19
EXP_B_RXP10_15]	EXP_B_RXP10_15]	19
EXP_B_RXN10_15]	EXP_B_RXN10_15]	19

## N.B HEATSINK



NB\_HS[12SP2-070018-01R, 12SP2-070018-02R]

HYPERTRANSPORT  
IF

HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
HT_TXCTL1P	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
HT_TXCTL1N	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
HT_TXCTL0P	P27	L0_CTLIN_H0	L0_CTLIN_H0	4
HT_TXCTL0N	P28	L0_CTLIN_L0	L0_CTLIN_L0	4
HT_TXCALP	D28	HT_TXCALP	NR1	1.21K/4/1
HT_TXCALN	D27	HT_TXCALN		

RD990/BGA692

20 PCIE4_4P	AD11	GPP3_RX9P	GPP3_RX9P	AG20
20 PCIE4_4N	AD11	GPP3_RX9N	GPP3_RX9N	AG20
20 PCIE4_3P	AD12	GPP3_RX8P	GPP3_RX8P	AG20
20 PCIE4_3N	AD12	GPP3_RX8N	GPP3_RX8N	AG20
20 PCIE4_2P	AD13	GPP3_RX7P	GPP3_RX7P	AG20
20 PCIE4_2N	AD13	GPP3_RX7N	GPP3_RX7N	AG20
20 PCIE4_1P	AD14	GPP3_RX6P	GPP3_RX6P	AG20
20 PCIE4_1N	AD14	GPP3_RX6N	GPP3_RX6N	AG20
32 RB_SL_IP	AD15	GPP3_RX5P	GPP3_RX5P	AG20
32 RB_SL_IN	AD15	GPP3_RX5N	GPP3_RX5N	AG20
33 UB_USB3_IN	AD16	GPP3_RX4P	GPP3_RX4P	AG20
33 UB_USB3_IN	AD16	GPP3_RX4N	GPP3_RX4N	AG20
19 PCIE4_4P_SB	AD17	GPP3_RX3P	GPP3_RX3P	AG20
19 PCIE4_4N_SB	AD17	GPP3_RX3N	GPP3_RX3N	AG20
19 PCIE4_3P_SB	AD18	GPP3_RX2P	GPP3_RX2P	AG20
19 PCIE4_3N_SB	AD18	GPP3_RX2N	GPP3_RX2N	AG20
19 PCIE4_2P_SB	AD19	GPP3_RX1P	GPP3_RX1P	AG20
19 PCIE4_2N_SB	AD19	GPP3_RX1N	GPP3_RX1N	AG20
19 PCIE4_1P_SB	AD20	GPP3_RX0P	GPP3_RX0P	AG20
19 PCIE4_1N_SB	AD20	GPP3_RX0N	GPP3_RX0N	AG20

14 A_RX3P	AC21	SB_RX3P	SB_RX3P	AG21
14 A_RX3N	AD21	SB_RX3N	SB_RX3N	AG21
14 A_RX2P	AE22	SB_RX2P	SB_RX2P	AG21
14 A_RX2N	AE22	SB_RX2N	SB_RX2N	AG21
14 A_RX1P	AG25	SB_RX1P	SB_RX1P	AG21
14 A_RX1N	AG25	SB_RX1N	SB_RX1N	AG21
14 A_RX0P	AG26	SB_RX0P	SB_RX0P	AG21
14 A_RX0N	AG26	SB_RX0N	SB_RX0N	AG21

NR2	1.27K/4/1	AE20	PCE_BCALRP	PCE_BCALRP
NR3	1.82K/4/1	AD20	PCE_BCALRN	PCE_BCALRN
NR4	1.27K/4/1	AE10	PCE_RCALRP	PCE_RCALRP
NR5	1.82K/4/1	AD10	PCE_RCALRN	PCE_RCALRN
NR6	1.27K/4/1	F14	PCE_TCALRP	PCE_TCALRP
NR7	1.82K/4/1	E14	PCE_TCALRN	PCE_TCALRN

20 PCIE4_4P	AD11	GPP3_RX9P	GPP3_RX9P	AG20
20 PCIE4_4N	AD11	GPP3_RX9N	GPP3_RX9N	AG20
20 PCIE4_3P	AD12	GPP3_RX8P	GPP3_RX8P	AG20
20 PCIE4_3N	AD12	GPP3_RX8N	GPP3_RX8N	AG20
20 PCIE4_2P	AD13	GPP3_RX7P	GPP3_RX7P	AG20
20 PCIE4_2N	AD13	GPP3_RX7N	GPP3_RX7N	AG20
20 PCIE4_1P	AD14	GPP3_RX6P	GPP3_RX6P	AG20
20 PCIE4_1N	AD14	GPP3_RX6N	GPP3_RX6N	AG20
32 RB_SL_IP	AD15	GPP3_RX5P	GPP3_RX5P	AG20
32 RB_SL_IN	AD15	GPP3_RX5N	GPP3_RX5N	AG20
33 UB_USB3_IN	AD16	GPP3_RX4P	GPP3_RX4P	AG20
33 UB_USB3_IN	AD16	GPP3_RX4N	GPP3_RX4N	AG20
19 PCIE4_4P_SB	AD17	GPP3_RX3P	GPP3_RX3P	AG20
19 PCIE4_4N_SB	AD17	GPP3_RX3N	GPP3_RX3N	AG20
19 PCIE4_3P_SB	AD18	GPP3_RX2P	GPP3_RX2P	AG20
19 PCIE4_3N_SB	AD18	GPP3_RX2N	GPP3_RX2N	AG20
19 PCIE4_2P_SB	AD19	GPP3_RX1P	GPP3_RX1P	AG20
19 PCIE4_2N_SB	AD19	GPP3_RX1N	GPP3_RX1N	AG20
19 PCIE4_1P_SB	AD20	GPP3_RX0P	GPP3_RX0P	AG20
19 PCIE4_1N_SB	AD20	GPP3_RX0N	GPP3_RX0N	AG20

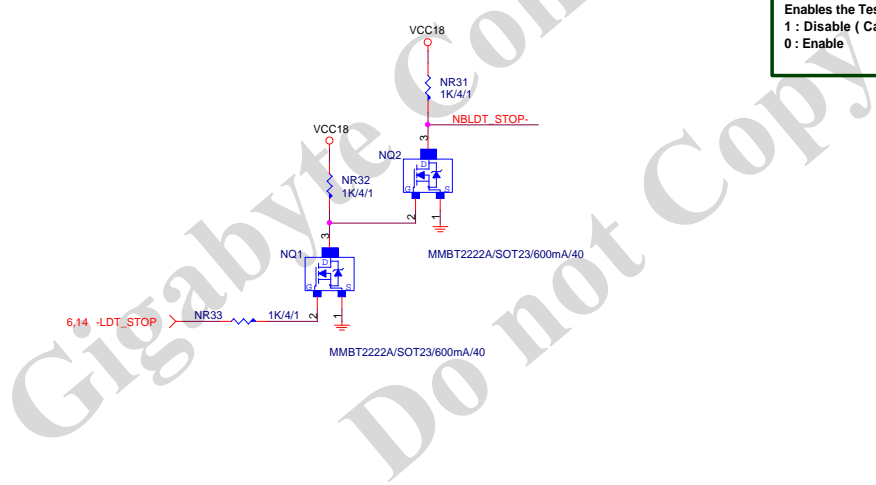
## PART 2/5

EXP_A_RXP15	N6	GPP1_RX15P	GPP1_RX15P	N3	EXP_A_TXP15
EXP_A_RXN15	N5	GPP1_RX15N	GPP1_RX15N	N2	EXP_A_TXN15
EXP_A_RXP14	M5	GPP1_RX14P	GPP1_RX14P	M2	EXP_A_TXP14
EXP_A_RXN14	M4	GPP1_RX14N	GPP1_RX14N	M1	EXP_A_TXN14
EXP_A_RXP13	L4	GPP1_RX13P	GPP1_RX13P	L3	EXP_A_TXP13
EXP_A_RXN13	L5	GPP1_RX13N	GPP1_RX13N	L2	EXP_A_TXN13
EXP_A_RXP12	K5	GPP1_RX12P	GPP1_RX12P	K2	EXP_A_TXP12
EXP_A_RXN12	K4	GPP1_RX12N	GPP1_RX12N	K1	EXP_A_TXN12
EXP_A_RXP11	J5	GPP1_RX11P	GPP1_RX11P	J3	EXP_A_TXP11
EXP_A_RXN11	J6	GPP1_RX11N	GPP1_RX11N	J2	EXP_A_TXN11
EXP_A_RXP10	H5	GPP1_RX10P	GPP1_RX10P	H2	EXP_A_TXP10
EXP_A_RXN10	H4	GPP1_RX10N	GPP1_RX10N	H1	EXP_A_TXN10
EXP_A_RXP9	G6	GPP1_RX9P	GPP1_RX9P	G3	EXP_A_TXP9
EXP_A_RXN9	G5	GPP1_RX9N	GPP1_RX9N	G2	EXP_A_TXN9
EXP_A_RXP8	F6	GPP1_RX8P	GPP1_RX8P	F2	EXP_A_TXP8
EXP_A_RXN8	F4	GPP1_RX8N	GPP1_RX8N	F1	EXP_A_TXN8
EXP_A_RXP7	D2	GPP1_RX7P	GPP1_RX7P	E3	EXP_A_TXP7
EXP_A_RXN7	D1	GPP1_RX7N	GPP1_RX7N	E2	EXP_A_TXN7
EXP_A_RXP6	B5	GPP1_RX6P	GPP1_RX6P	A4	EXP_A_TXP6
EXP_A_RXN6	C5	GPP1_RX6N	GPP1_RX6N	B4	EXP_A_TXN6
EXP_A_RXP5	B6	GPP1_RX5P	GPP1_RX5P	A6	EXP_A_TXP5
EXP_A_RXN5	E6	GPP1_RX5N	GPP1_RX5N	B6	EXP_A_TXN5
EXP_A_RXP4	E7	GPP1_RX4P	GPP1_RX4P	B7	EXP_A_TXP4
EXP_A_RXN4	D7	GPP1_RX4N	GPP1_RX4N	C7	EXP_A_TXN4
EXP_A_RXP3	E8	GPP1_RX3P	GPP1_RX3P	A8	EXP_A_TXP3
EXP_A_RXN3	E8	GPP1_RX3N	GPP1_RX3N	B8	EXP_A_TXN3
EXP_A_RXP2	E9	GPP1_RX2P	GPP1_RX2P	B9	EXP_A_TXP2
EXP_A_RXN2	E9	GPP1_RX2N	GPP1_RX2N	C3	EXP_A_TXN2
EXP_A_RXP1	E10	GPP1_RX1P	GPP1_RX1P	A10	EXP_A_TXP1
EXP_A_RXN1	E10	GPP1_RX1N	GPP1_RX1N	B10	EXP_A_TXN1
EXP_A_RXP0	E11	GPP1_RX0P	GPP1_RX0P	B11	EXP_A_TXP0
EXP_A_RXN0	F11	GPP1_RX0N	GPP1_RX0N	C11	EXP_A_TXN0

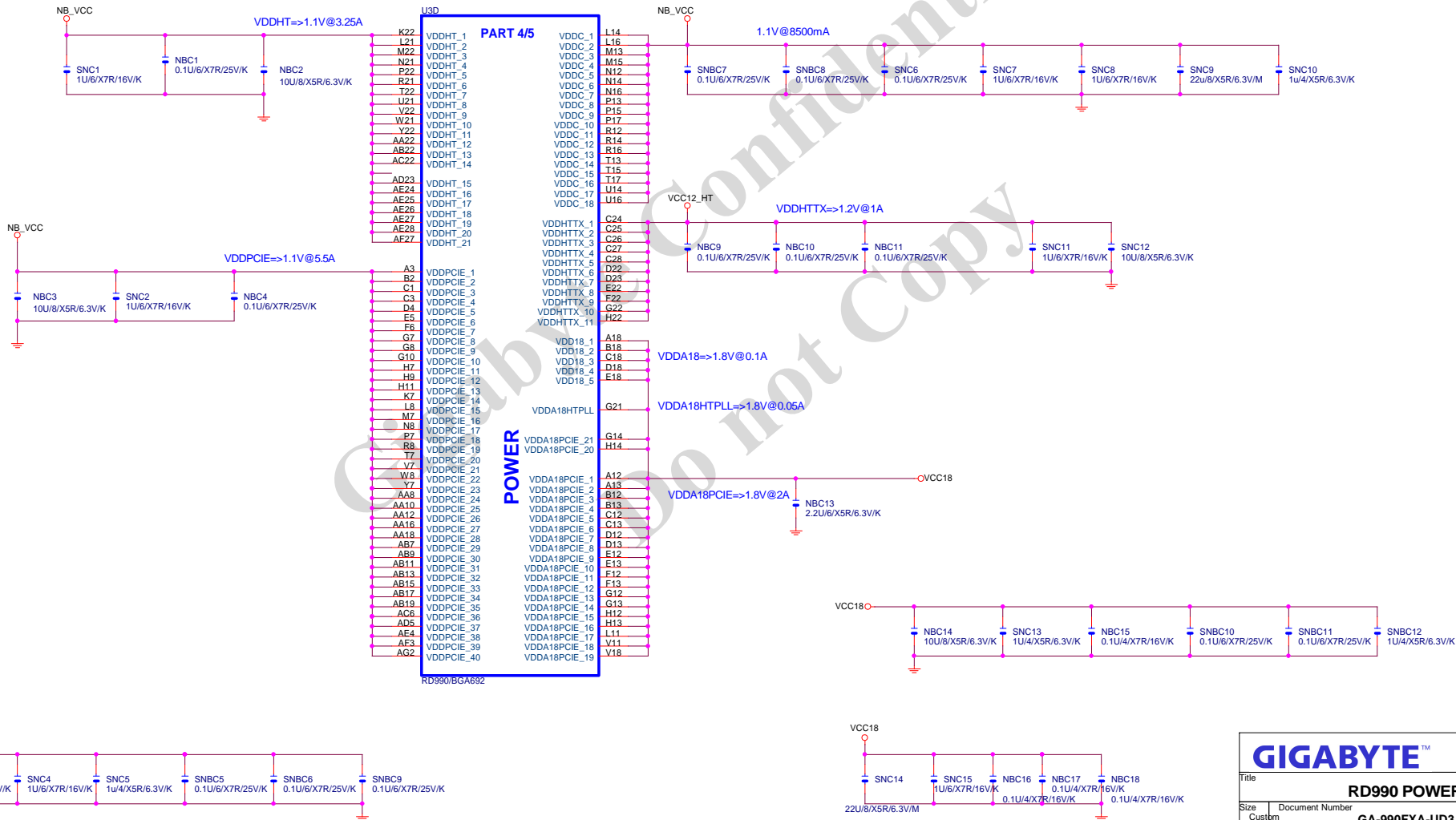
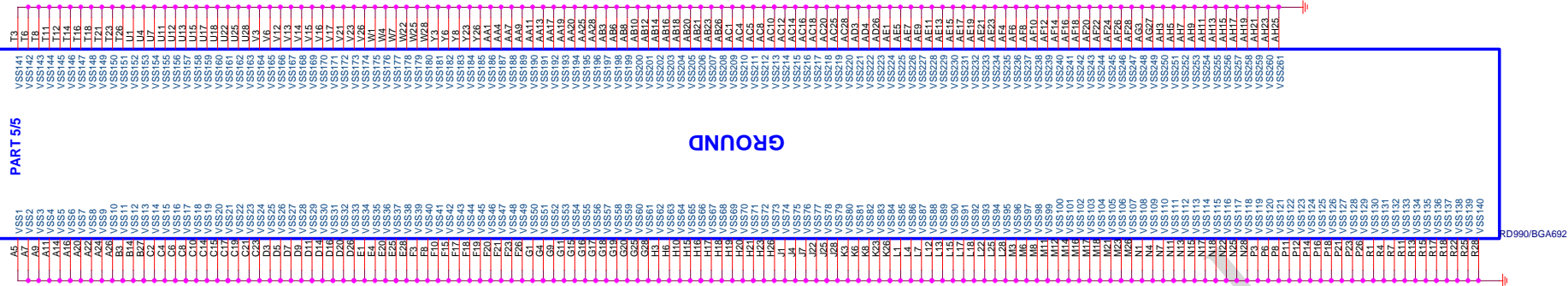
EXP_B_RXP15	AC9	GPP2_RX15P	GPP2_RX15P	AF9	EXP_B_TXP15
EXP_B_RXN15	AD9	GPP2_RX15N	GPP2_RX15N	AG9	EXP_B_TXN15
EXP_B_RXP14	AE8	GPP2_RX14P	GPP2_RX14P	AH8	EXP_B_TXP14
EXP_B_RXN14	AE8	GPP2_RX14N	GPP2_RX14N	AH7	EXP_B_TXN14
EXP_B_RXP13	AC7	GPP2_RX13P	GPP2_RX13P	AF7	EXP_B_TXP13
EXP_B_RXN13	AD7	GPP2_RX13N	GPP2_RX13N	AG7	EXP_B_TXN13
EXP_B_RXP12	AD6	GPP2_RX12P	GPP2_RX12P	AG6	EXP_B_TXP12
EXP_B_RXN12	AE6	GPP2_RX12N	GPP2_RX12N	AH6	EXP_B_TXN12
EXP_B_RXP11	AE5	GPP2_RX11P	GPP2_RX11P	AG4	EXP_B_TXP11
EXP_B_RXN11	AG5	GPP2_RX11N	GPP2_RX11N	AH4	EXP_B_TXN11
EXP_B_RXP10	AE2	GPP2_RX10P	GPP2_RX10P	AE3	EXP_B_TXP10
EXP_B_RXN10	AE1	GPP2_RX10N	GPP2_RX10N	AE2	EXP_B_TXN10
EXP_B_RXP9	AD2	GPP2_RX9P	GPP2_RX9P	AC3	EXP_B_TXP9
EXP_B_RXN9	AD1	GPP2_RX9N	GPP2_RX9N	AC2	EXP_B_TXN9
EXP_B_RXP8	AB5	GPP2_RX8P	GPP2_RX8P	AB2	EXP_B_TXP8
EXP_B_RXN8	AB4	GPP2_RX8N	GPP2_RX8N	AB1	EXP_B_TXN8
EXP_B_RXP7	AA6	GPP2_RX7P	GPP2_RX7P	AA3	EXP_B_TXP7
EXP_B_RXN7	AA5	GPP2_RX7N	GPP2_RX7N	AA2	EXP_B_TXN7
EXP_B_RXP6	Y5	GPP2_RX6P	GPP2_RX6P	Y2	EXP_B_TXP6
EXP_B_RXN6	Y4	GPP2_RX6N	GPP2_RX6N	Y1	EXP_B_TXN6
EXP_B_RXP5	W6	GPP2_RX5P	GPP2_RX5P	W3	EXP_B_TXP5
EXP_B_RXN5	W5	GPP2_RX5N	GPP2_RX5N	W2	EXP_B_TXN5
EXP_B_RXP4	V5	GPP2_RX4P	GPP2_RX4P	V2	EXP_B_TXP4
EXP_B_RXN4	V4	GPP2_RX4N	GPP2_RX4N	V1	EXP_B_TXN4
EXP_B_RXP3	U6	GPP2_RX3P	GPP2_RX3P	U3	EXP_B_TXP3
EXP_B_RXN3	U5	GPP2_RX3N	GPP2_RX3N	U2	EXP_B_TXN3
EXP_B_RXP2	T5	GPP2_RX2P	GPP2_RX2P	T2	EXP_B_TXP2
EXP_B_RXN2	T4	GPP2_RX2N	GPP2_RX2N	T1	EXP_B_TXN2
EXP_B_RXP1	RE	GPP2_RX1P	GPP2_RX1P	R3	EXP_B_TXP1
EXP_B_RXN1	RE	GPP2_RX1N	GPP2_RX1N	R2	EXP_B_TXN1
EXP_B_RXP0	P4	GPP2_RX0P	GPP2_RX0P	P2	EXP_B_TXP0
EXP_B_RXN0	P4	GPP2_RX0N	GPP2_RX0N	P1	EXP_B_TXN0

AD11	GPP3_RX9P
AD11	GPP3_RX9N
AE12	GPP3_RX8P
AD12	GPP3_RX8N
AD13	GPP3_RX7P
AC13	GPP3_RX7N
AE14	GPP3_RX6P
AD14	GPP3_RX6N
AD15	GPP3_RX5P
AC15	GPP3_RX5N
AE16	GPP3_RX4P
AD16	GPP3_RX4N
AD17	GPP3_RX3P
AC17	GPP3_RX3N
AE18	GPP3_RX2P
AD18	GPP3_RX2N
AD19	GPP3_RX1P
AC19	GPP3_RX1N
AH20	GPP3_RX0P
AG20	GPP3_RX0N

PCIE GPP3E GPP2



Enables the Test Debug Bus using PCIe bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

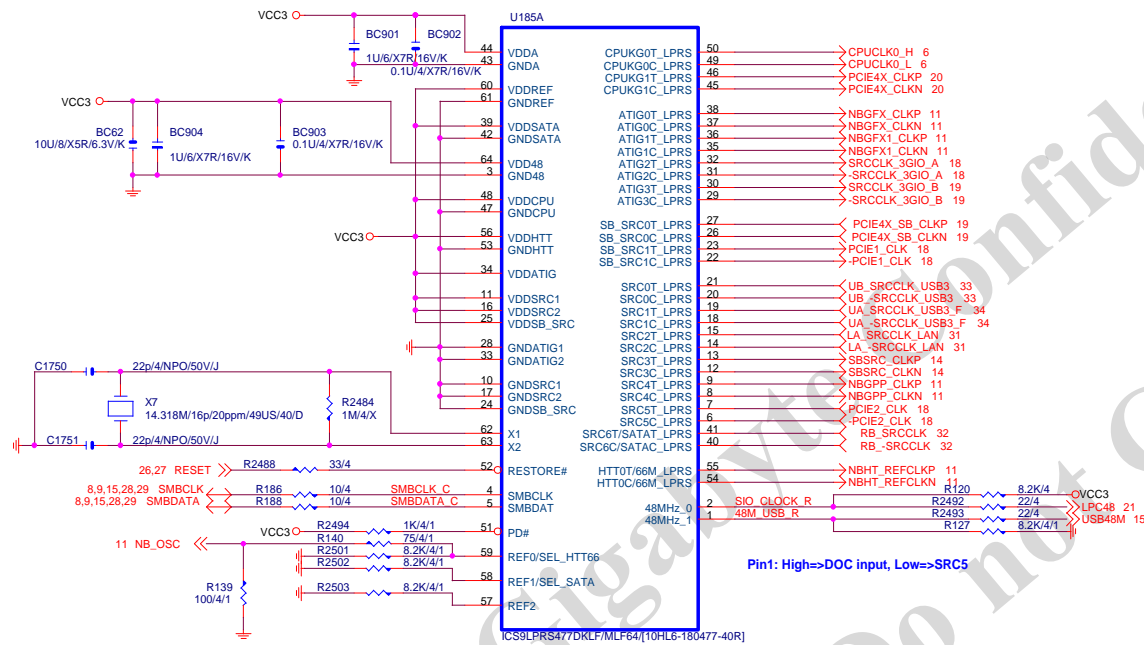
**GIGABYTE™**Title **RD990 POWER**Size Document Number **GA-990FXA-UD3** Rev **1.11**

Date: Monday, May 07, 2012 Sheet 12 of 35

## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

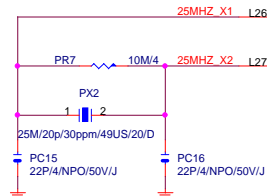
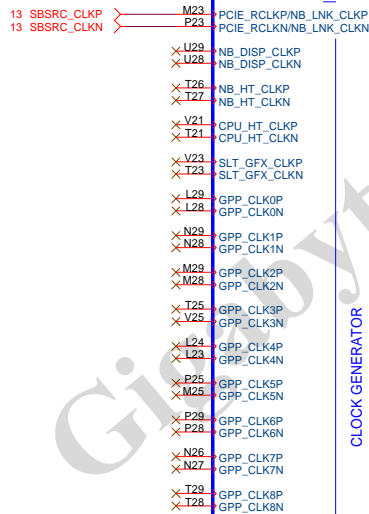
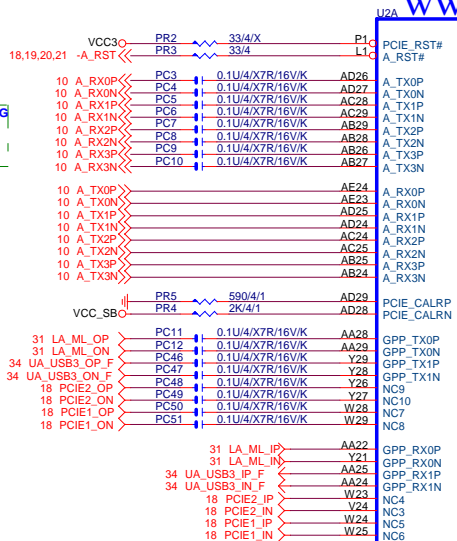
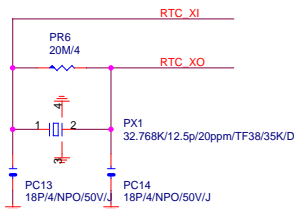
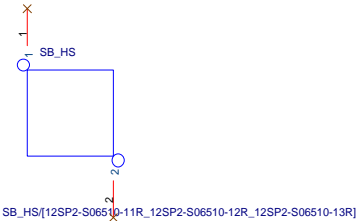
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

Title	ICS9LPRS477		
Size	Document Number	GA-990FXA-UD3	
Custom			Rev 1.11
Date:	Monday, May 07, 2012	Sheet 13	of 35

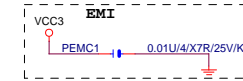
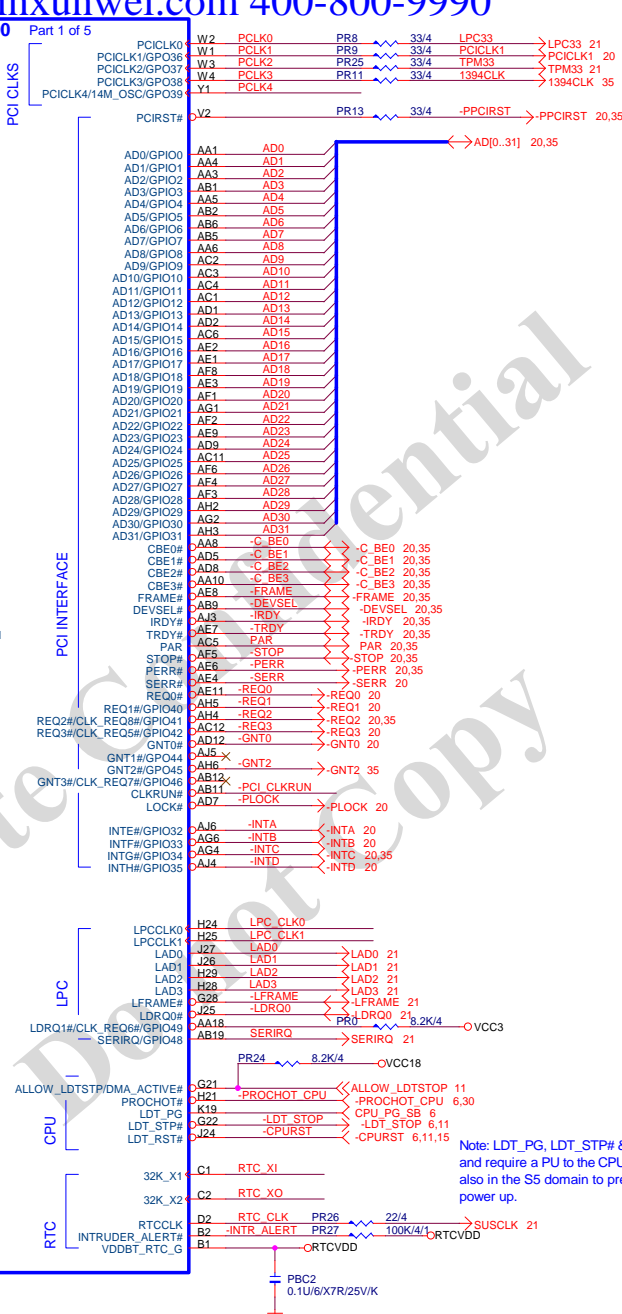
S.B HEATSINK



## PCI EXPRESS INTERFACES

## PCI INTERFACE

## CLOCK GENERATOR

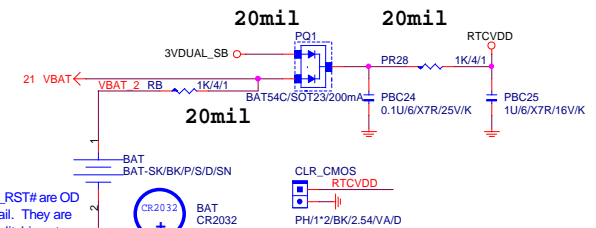


Low: Force PCIE GEN1, Up: Allow PCIE GEN2

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting  
EC AOD-ACC

	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

**GIGABYTE™**

Title			
ATi SB950 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	1.11	
Date:	Monday, May 07, 2012	Sheet	14 of 35



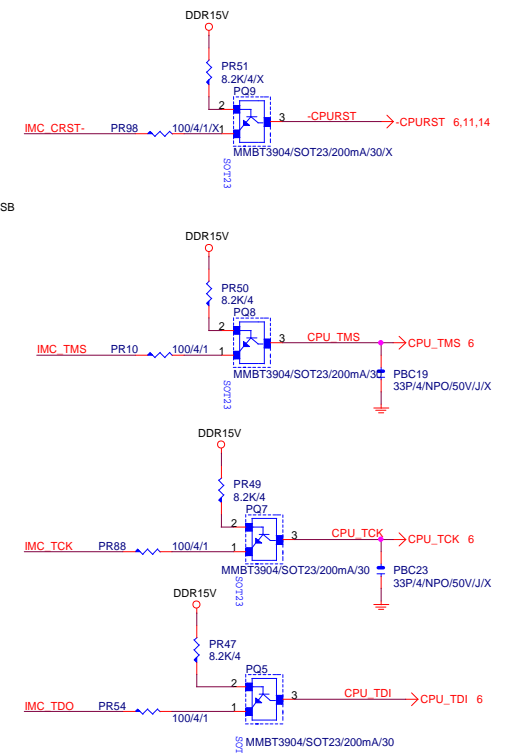
USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR\_GD signals  
can be used for power-up sequencer

IMC\_GPIO200 PR61 2.2K/4/1  
IMC\_GPIO199 PR62 2.2K/4/1

IMC\_GPIO200 IMC\_GPIO199

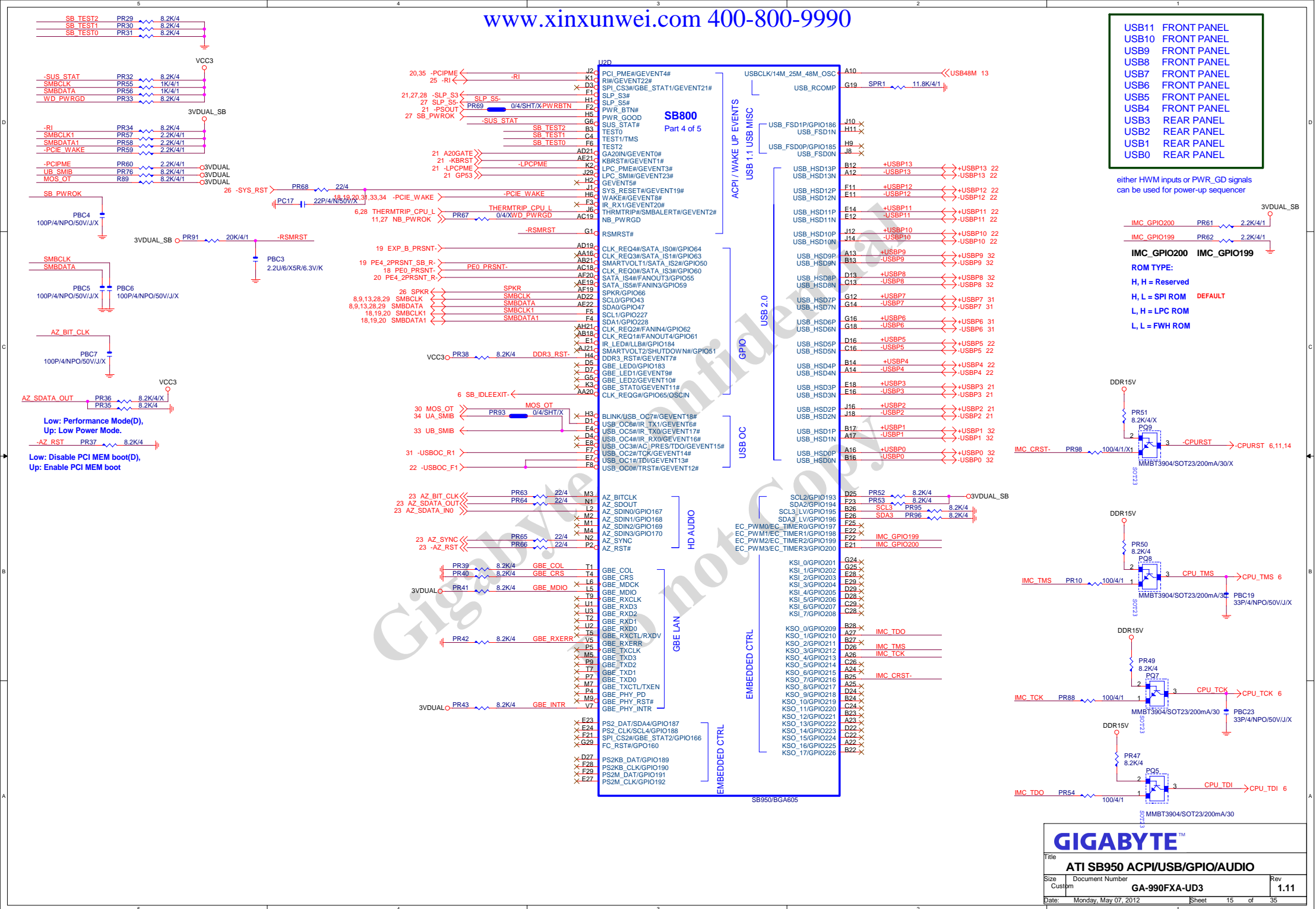
ROM TYPE:  
H, H = Reserved  
L, L = SPI ROM DEFAULT  
L, H = LPC ROM  
L, L = FWH ROM



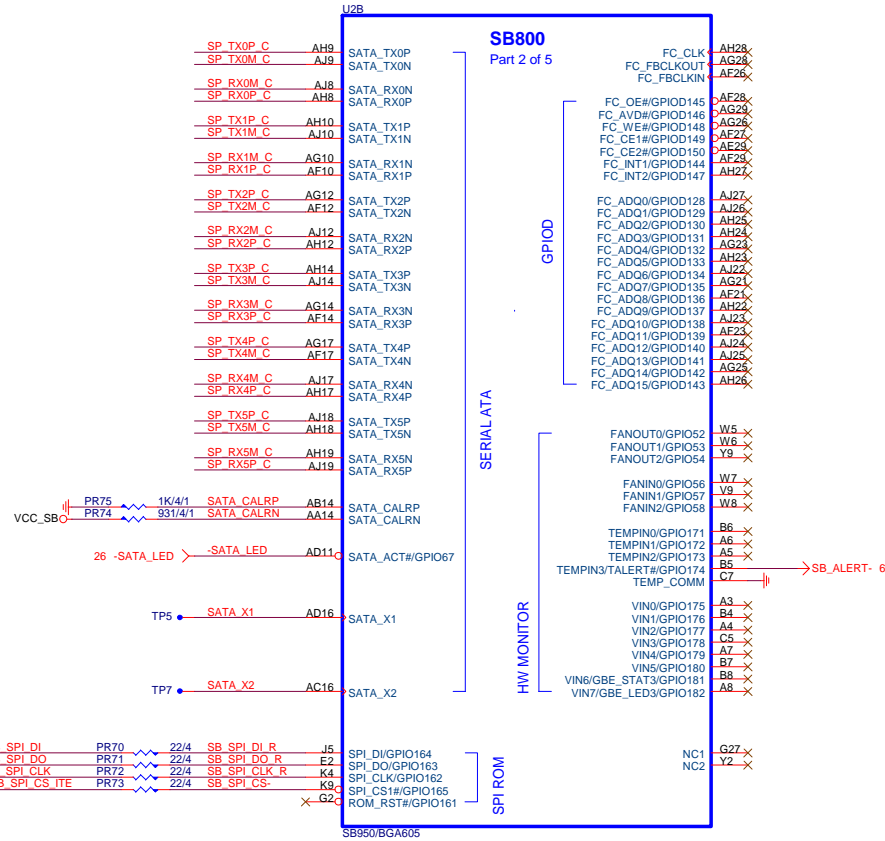
# GIGABYTE

ATI SB950 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-990FXA-UD3	1.11
Date:	Monday, May 07, 2012	Sheet 15 of 35







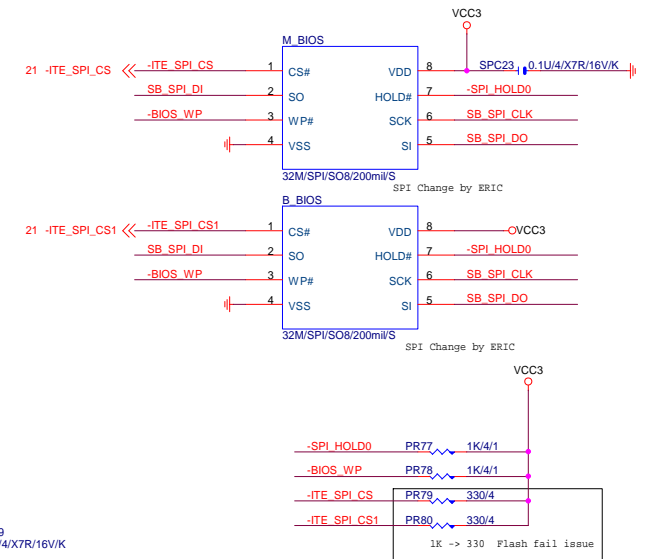
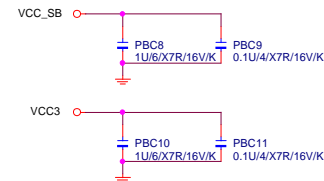
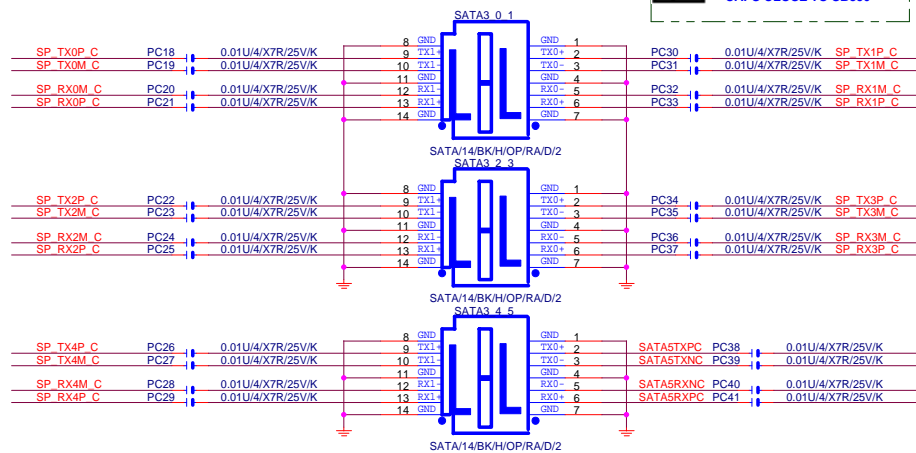
PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF U600

#### NOTE:

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850



**GIGABYTE**

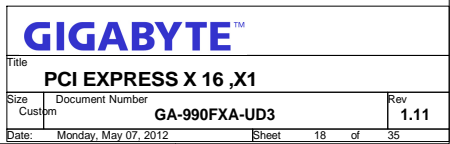
Title	ATI SB950 SATA/IDE/HWM/SPI		
Size	Document Number	Rev	1.11
Custm	GA-990FXA-UD3		
Date:	Monday, May 07, 2012	Sheet	16 of 35

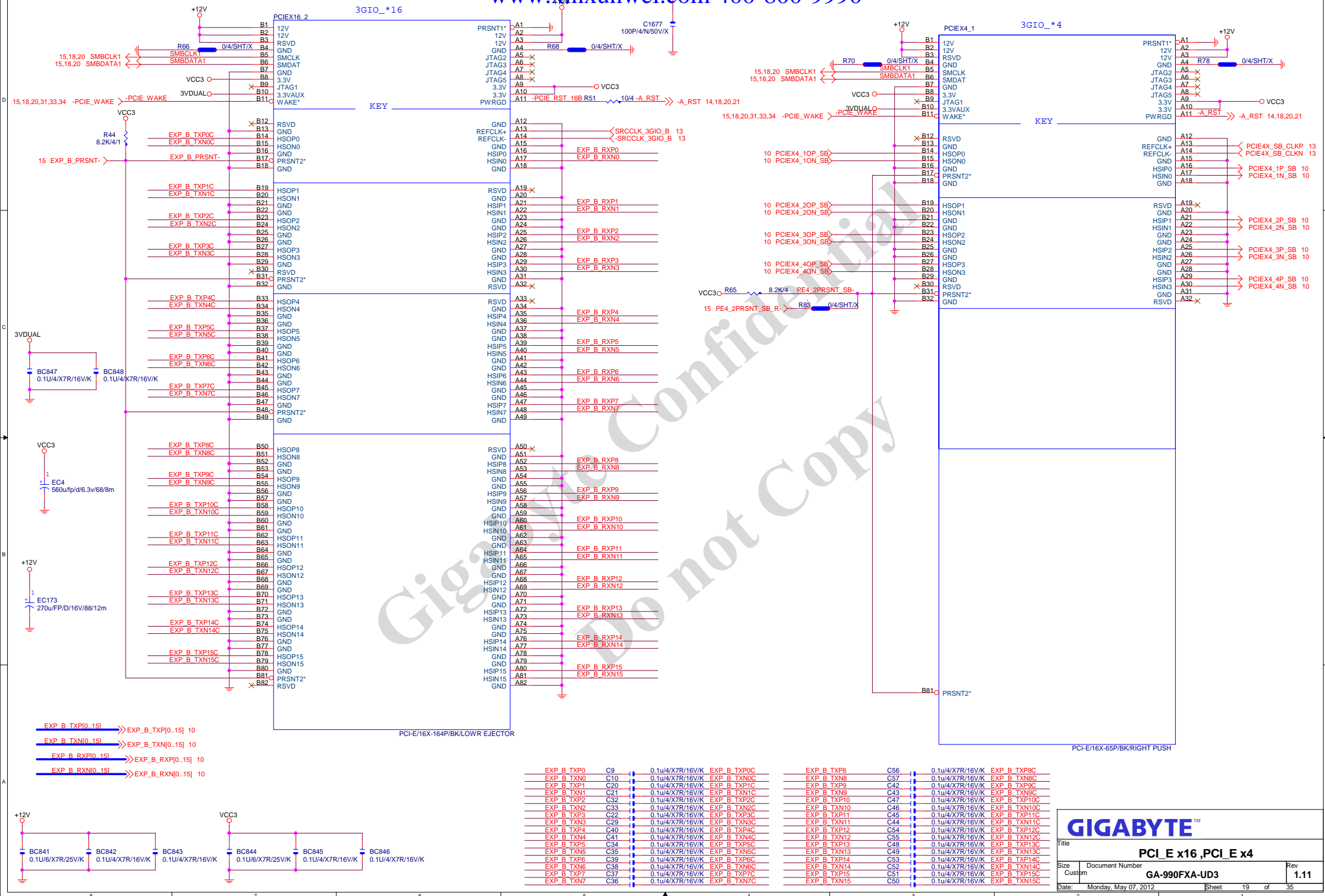
[illegible]

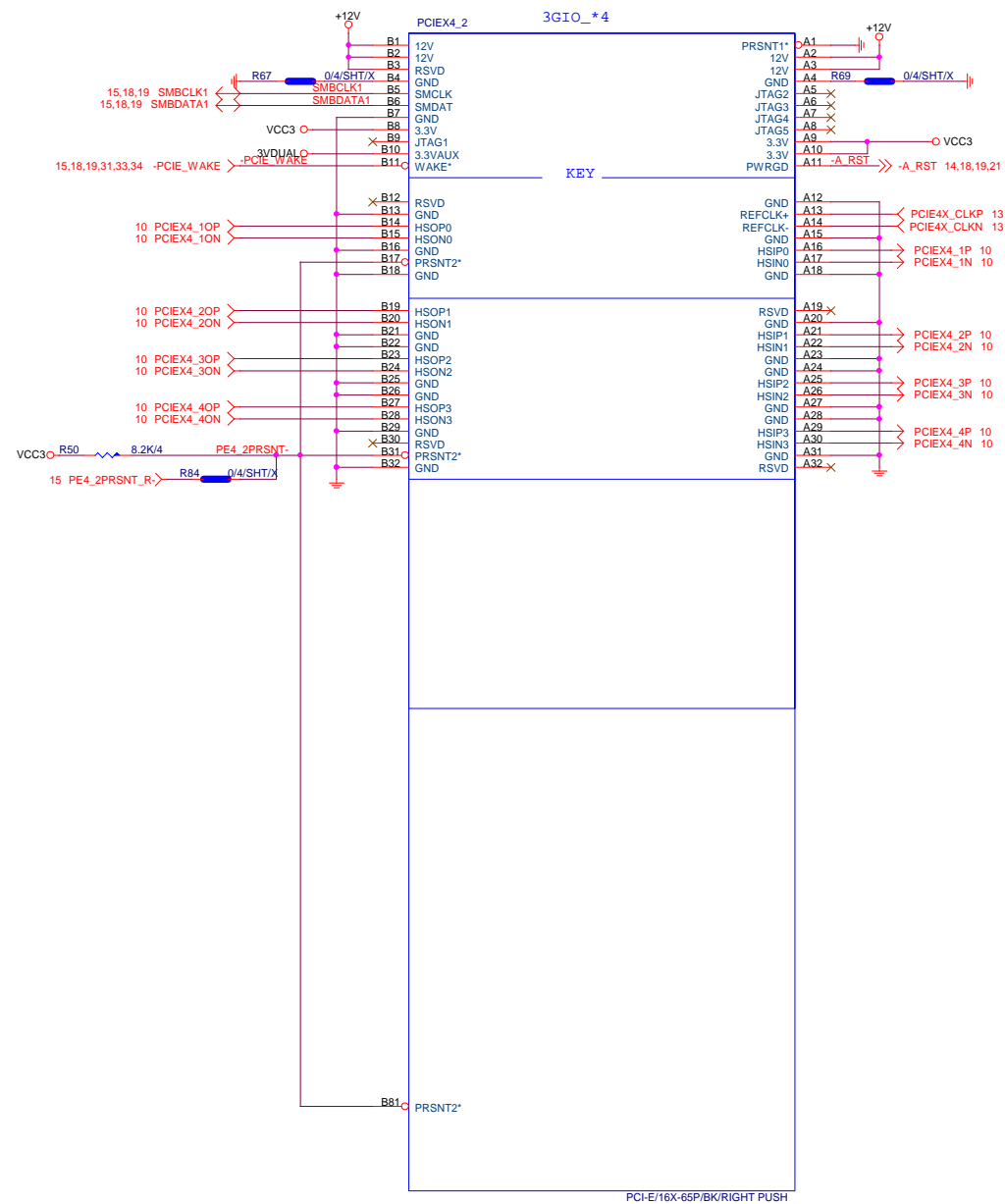
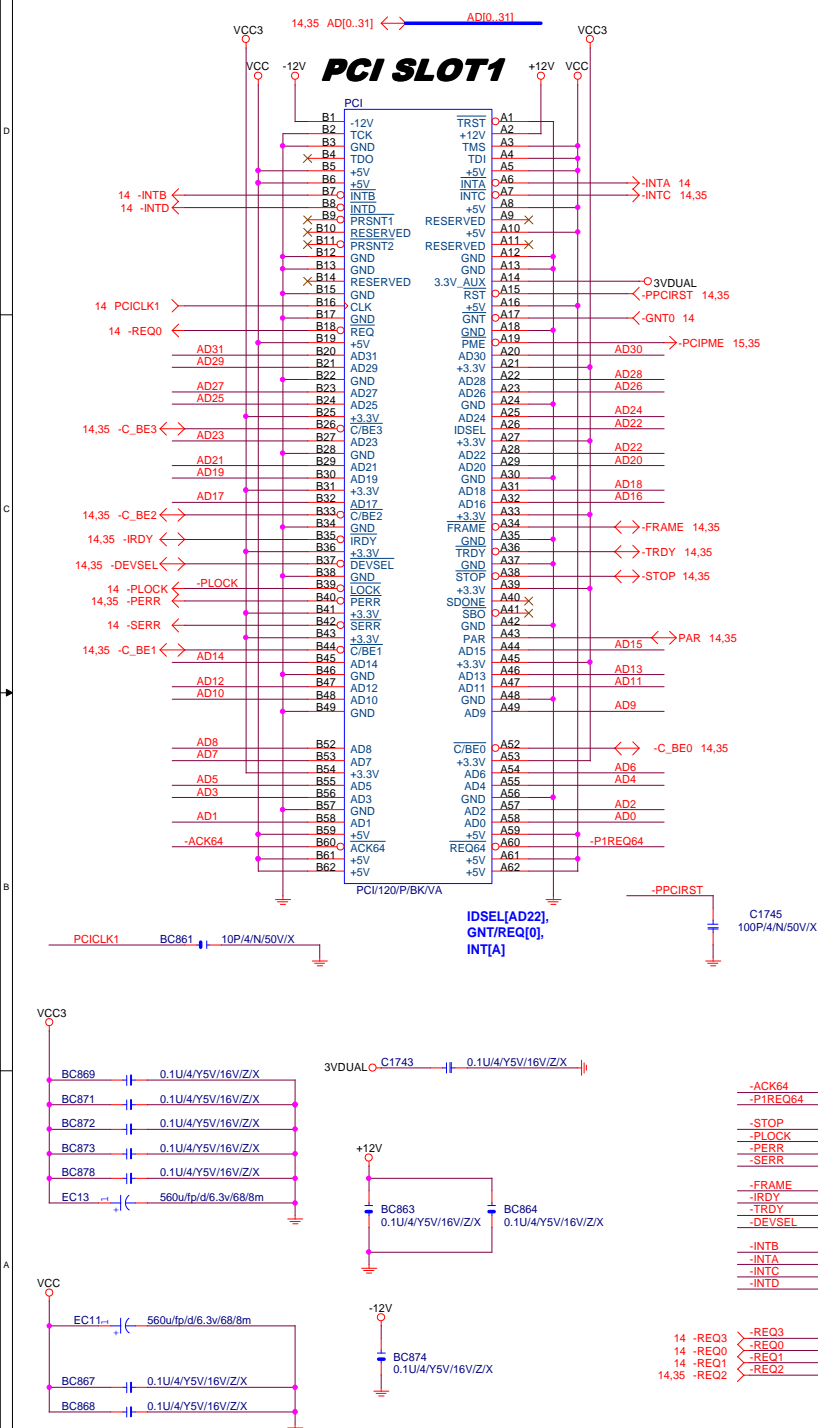
Part 5 of 5

SB950/BGA605

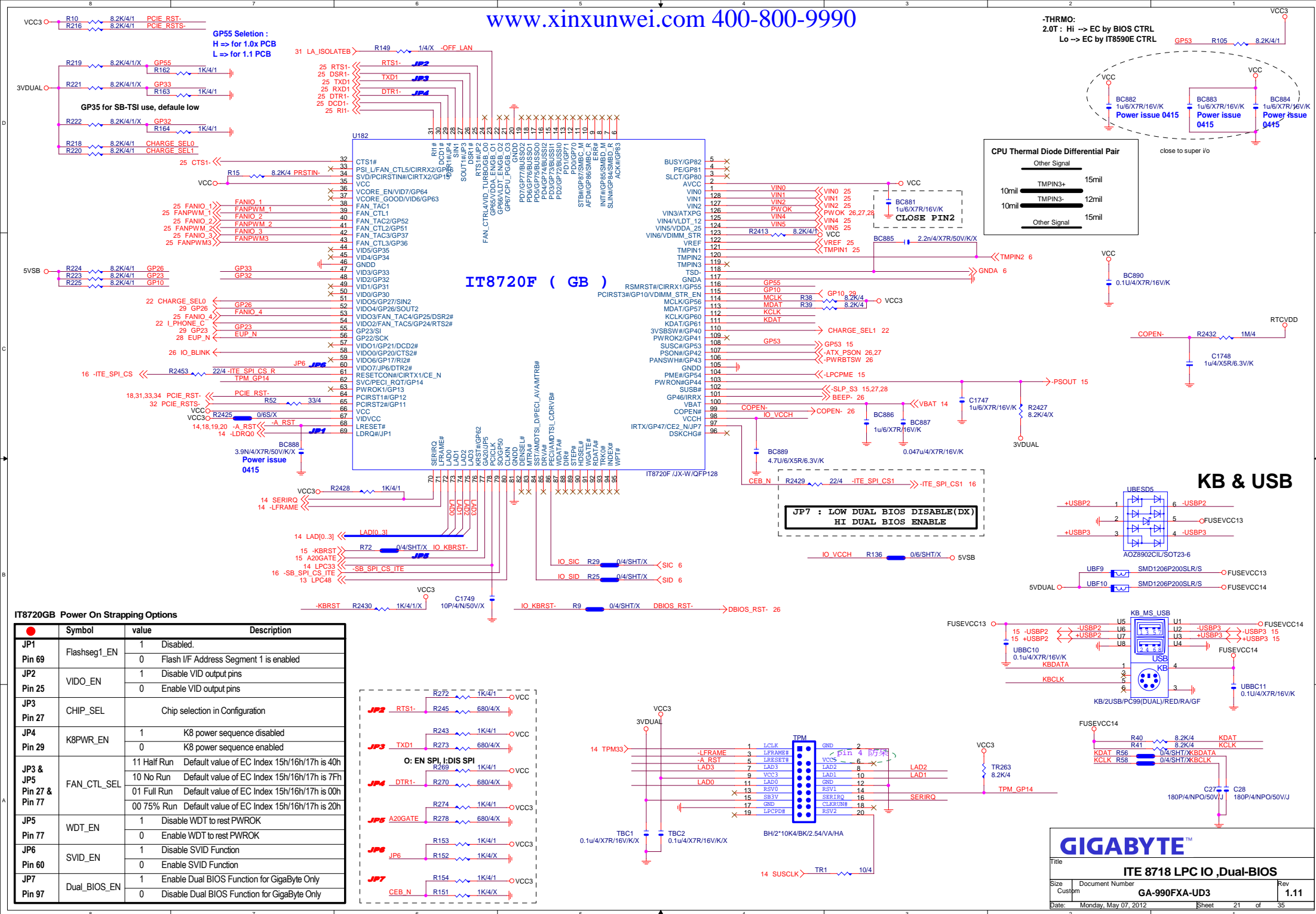
Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>1.11</b>
Date: Monday, May 07, 2012	Sheet 17 of 35	





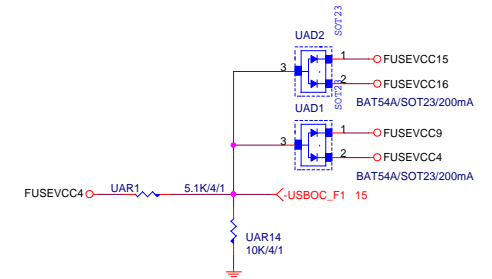
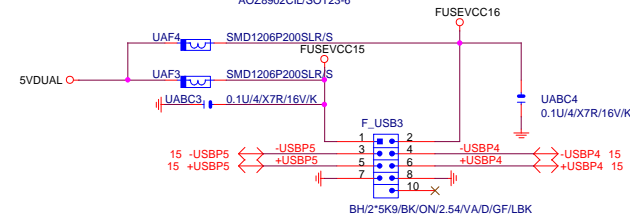
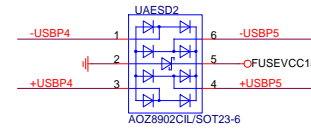
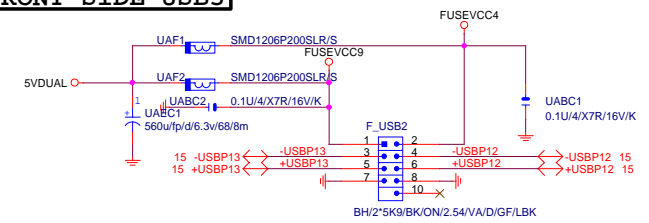
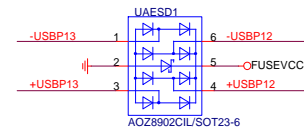
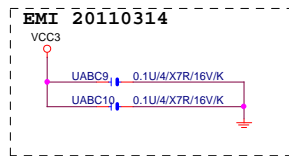


-THRMO:  
2.0T : HI --> EC by BIOS CTRL  
Lo --> EC by IT8590E CTRL

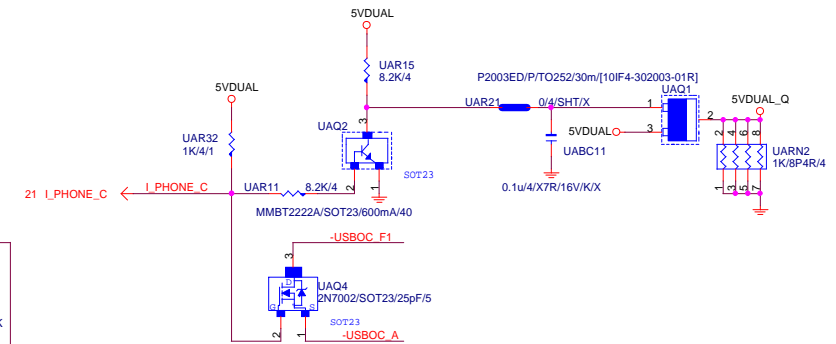
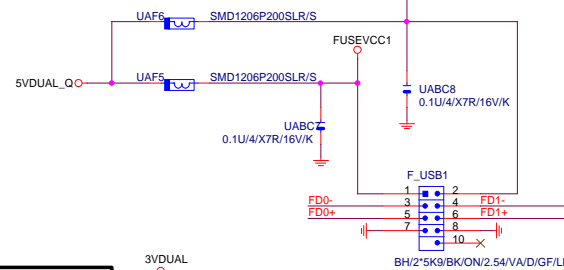




## FRONT SIDE USB3

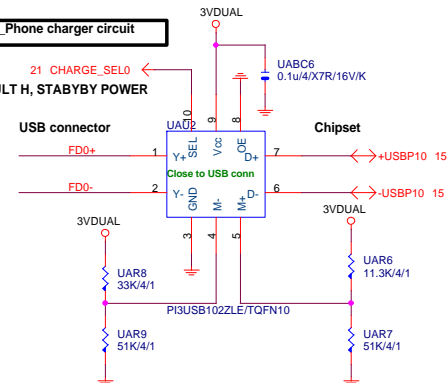


## FRONT SIDE USB1

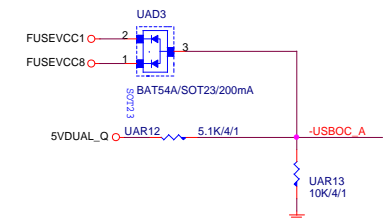
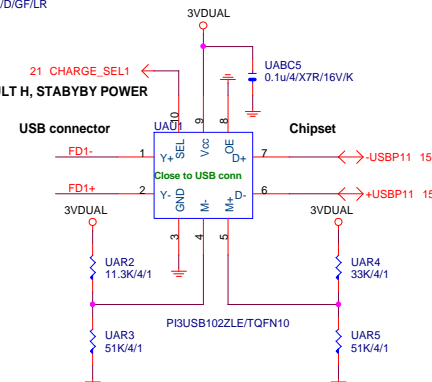


## i\_Phone charger circuit

21 CHARGE\_SEL0  
DEFAULT H, STABBY POWER



21 CHARGE\_SEL1  
DEFAULT H, STABBY POWER

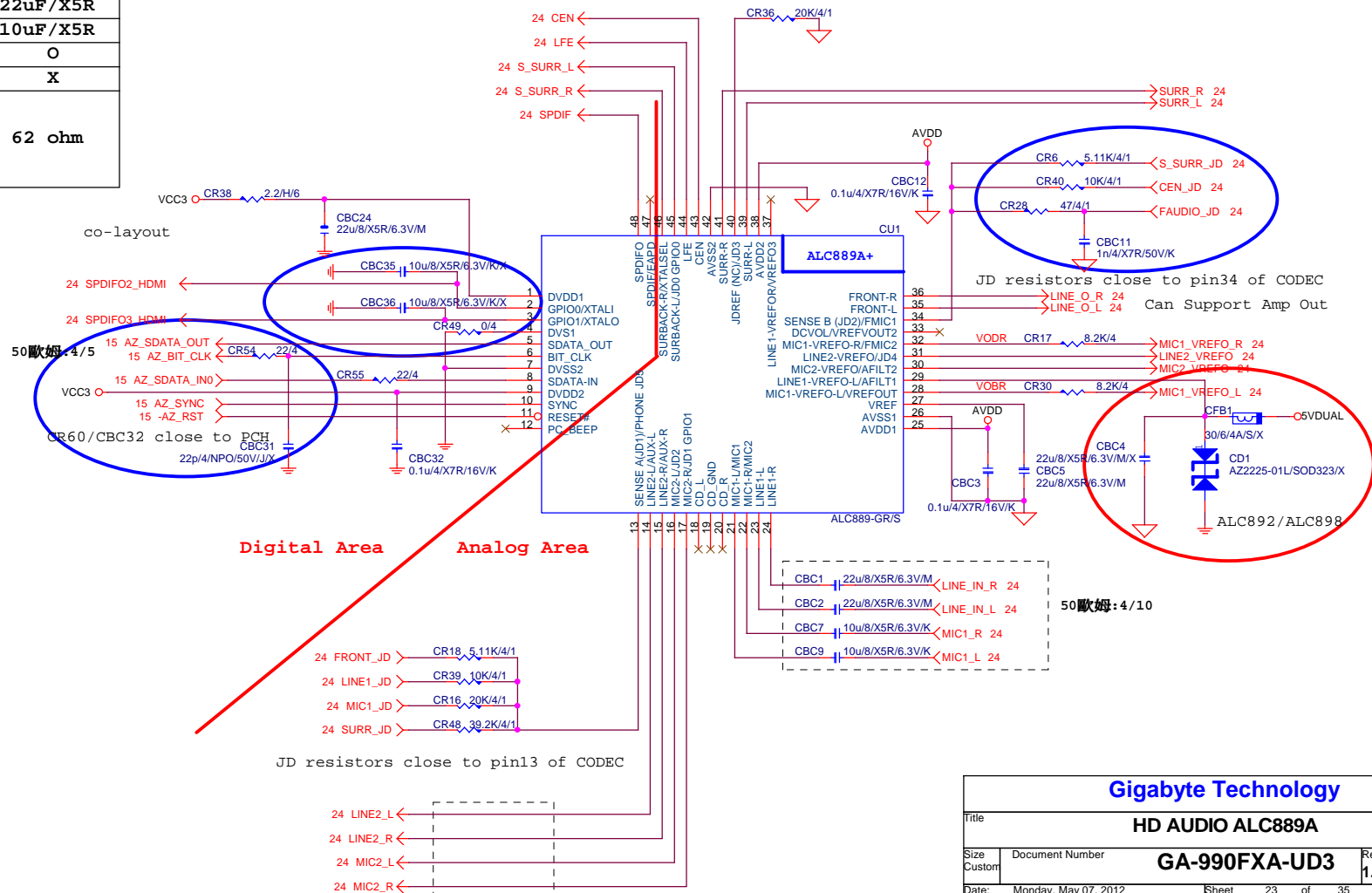


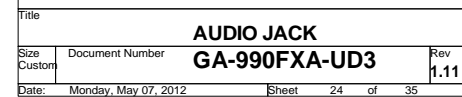
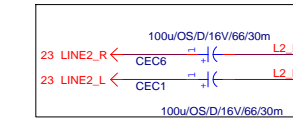
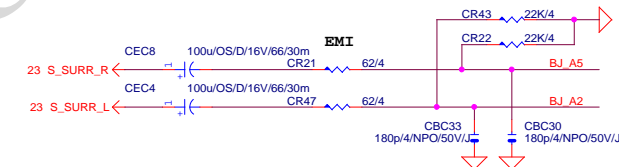
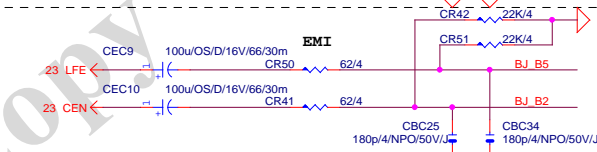
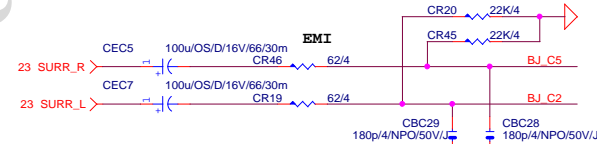
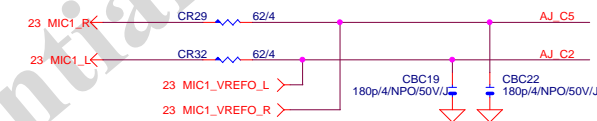
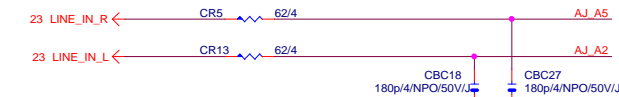
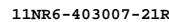
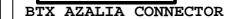
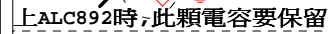
**GIGABYTE**

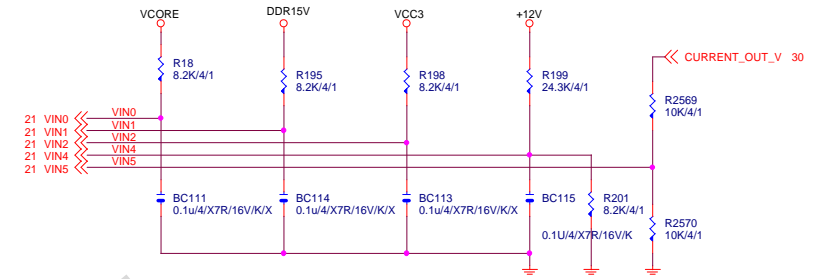
Title					
COM/LPT/F_USB					
Size	Document Number				Rev
Custom	GA-990FXA-UD3				1.11
Date:	Monday, May 07, 2012		Sheet	22 of	35



	ALC889	ALC889B	ALC898/ALC892
CR65	O	O	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	O	X	O
CR66	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	O
CD2/CD3/CQ3/CQ5	O	O	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm







Pin connection diagram for the DAU1 module. The diagram shows a central DAU1 module with pins 1 through 20. On the left, pins 1-19 are connected to a 12V source through resistors. On the right, pins 2-20 are connected to a 12V source through resistors. The bottom of the diagram shows three capacitors (OABC1, OABC2, OABC3) connected to ground.

Pin	Signal	Pin	Signal
1	R11-	2	NRIA-
2	CTS1-	3	NCTSA-
3	DSR1-	4	NRSA-
4	RTS0	5	NTRSA-
5	DTR1-	6	NDTRA-
6	RXD1	7	NSINA-
7	TXD1	8	NSLUTA
8	DCD1-	9	NDCCA-
9		10	
10		11	
11		12	
12		13	
13		14	
14		15	
15		16	
16		17	
17		18	
18		19	
19		20	

12V

GND

5V

12V

VCC

+12V

OABC1

OABC3

OABC2

0.1u4/X7R/16V/K/X

GD75232/TSSOP20

0.1u4/X7R/16V/K/X

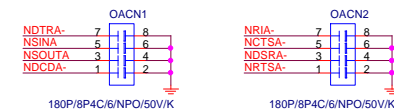
0.1u4/X7R/16V/K/X

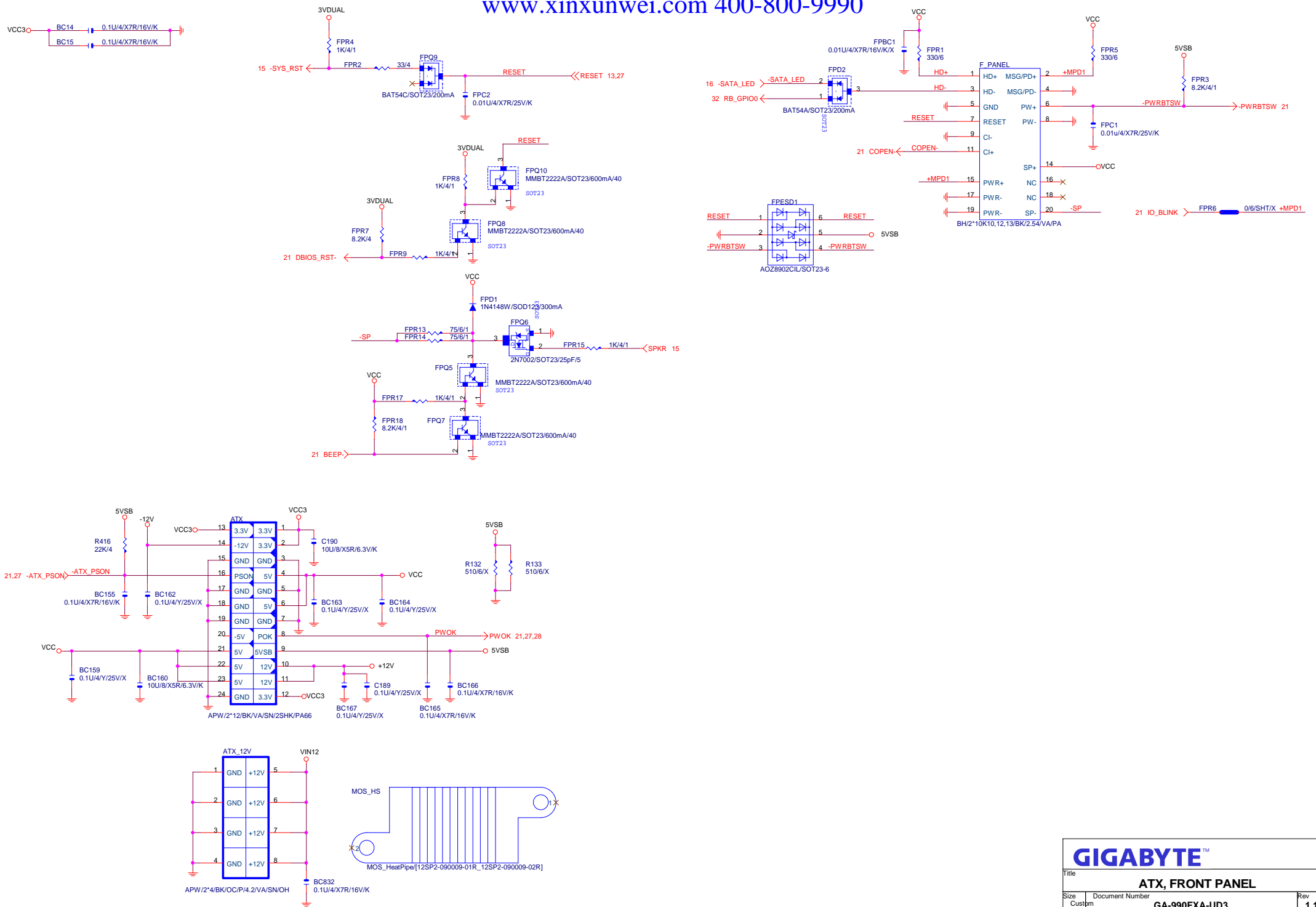
[illegible]

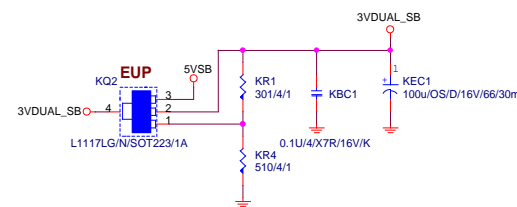
Figure 1: Schematic representation of the 10 genes analyzed. The diagram shows 10 horizontal lines representing genes, numbered 1 to 10. Lines 1-4 are on the left, and lines 5-10 are on the right. Lines 1-4 are labeled NDCDA-, NSOUTA, NRTSA-, and NR1A- respectively. Lines 5-10 are labeled NSINA, NDTRA-, NDSRA-, and NCTSA- respectively. A vertical line separates the two groups. A small 'v' symbol is at the end of line 10.

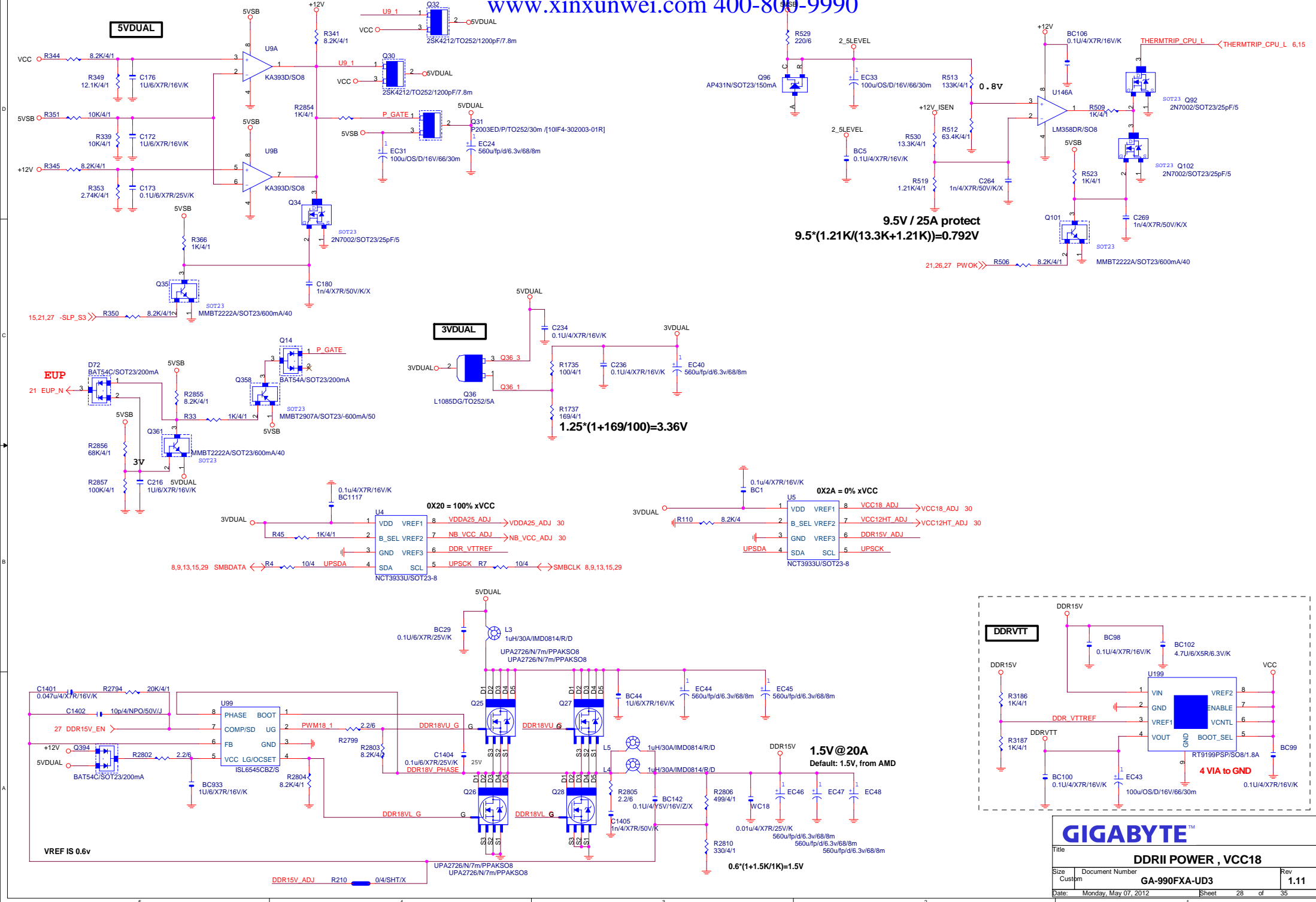
BH/2\*5K10/BK/2.54/VA/COM

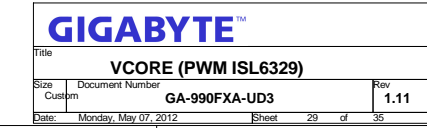
11NH3-000205-Y1R/Y2R



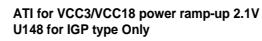
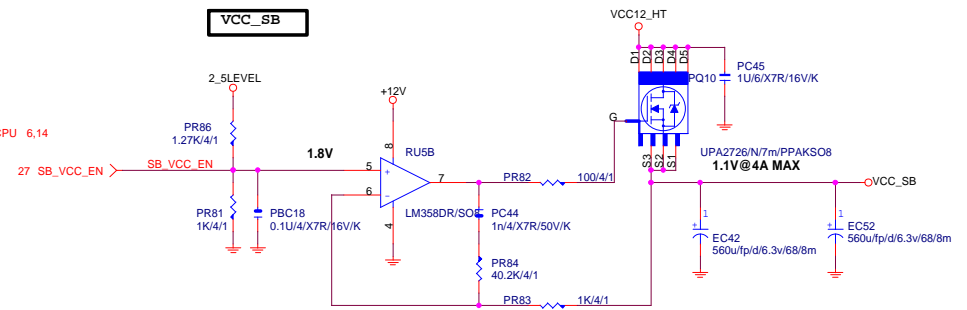
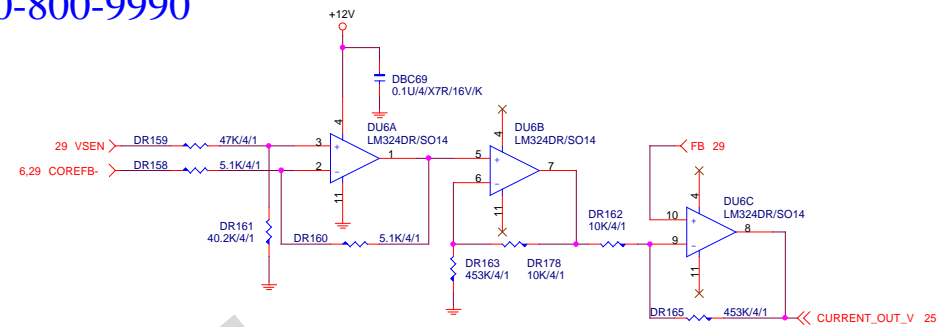




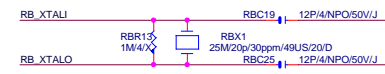
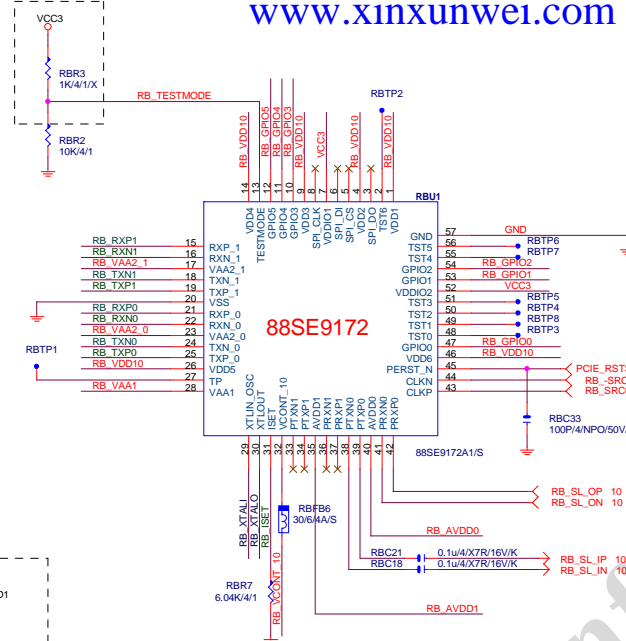
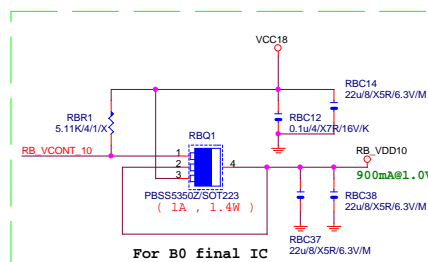
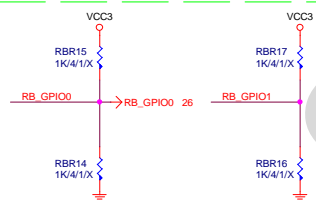
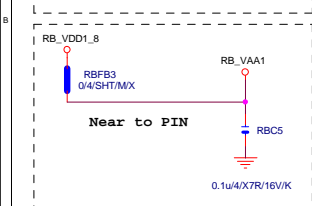
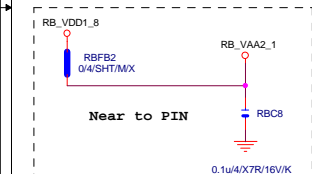
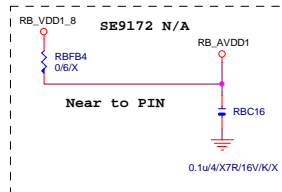
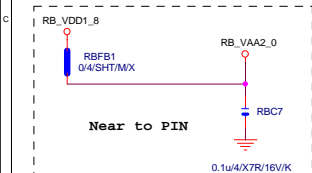
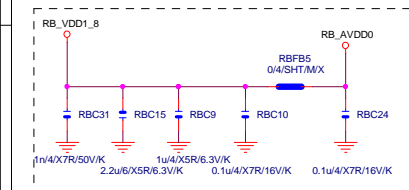
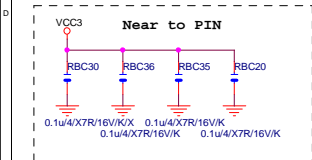
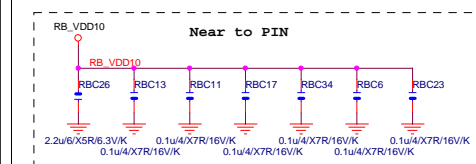




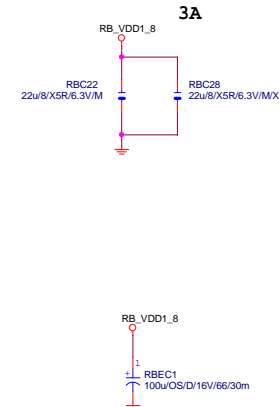
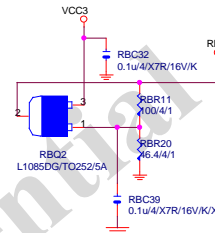




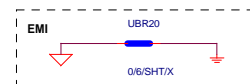
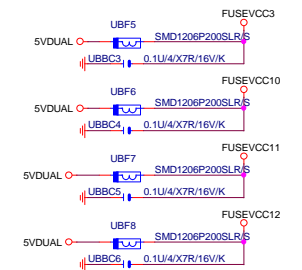
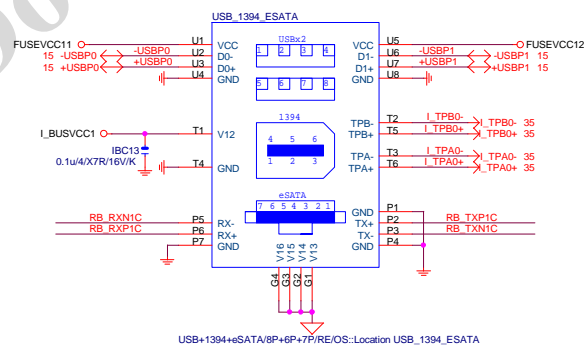
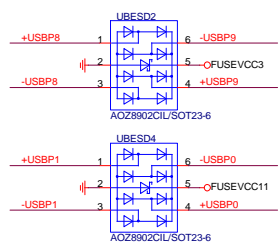
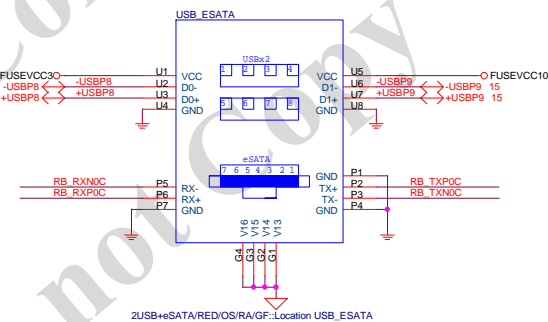
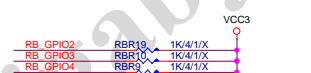


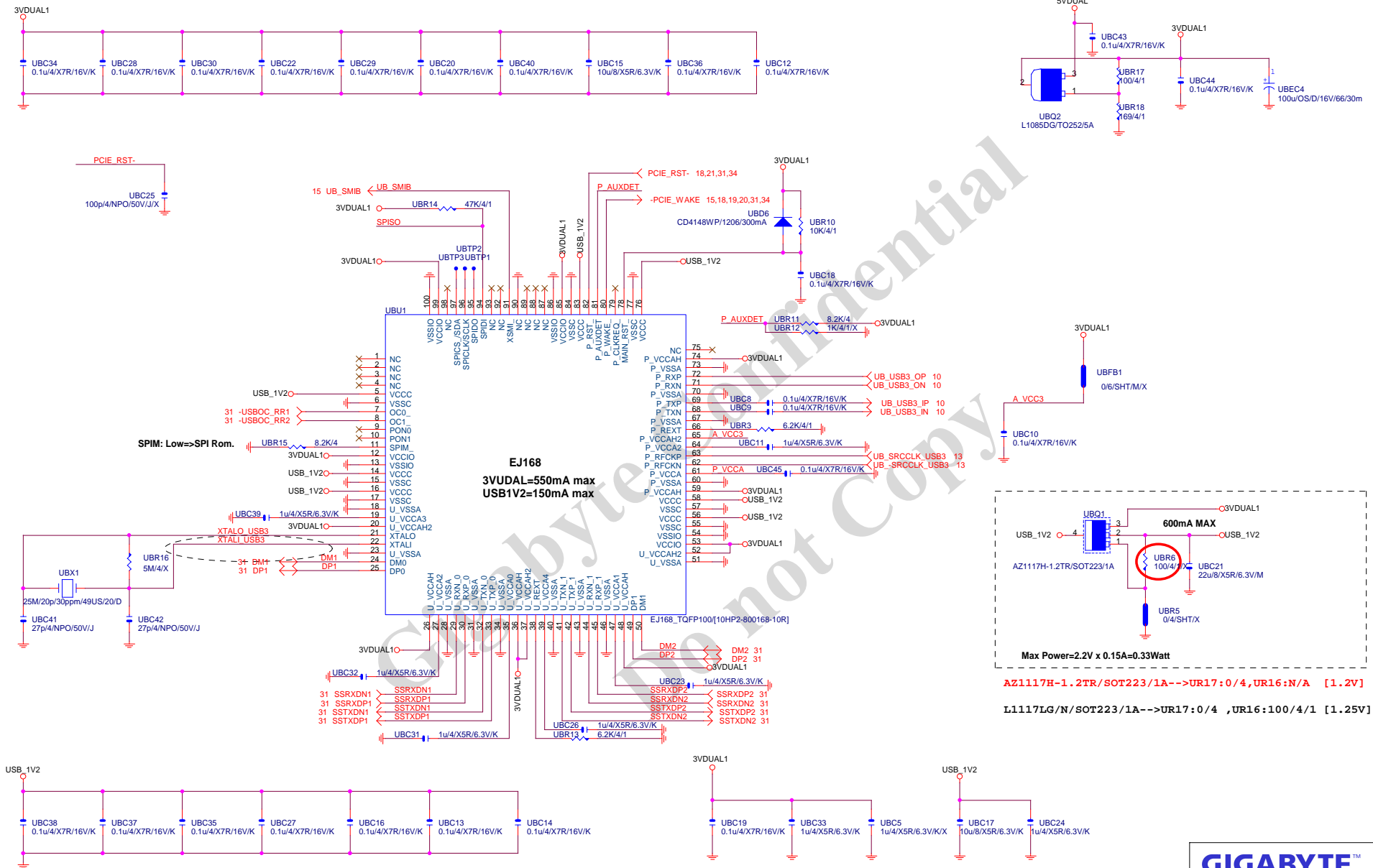


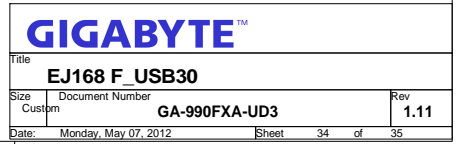
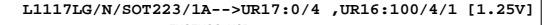
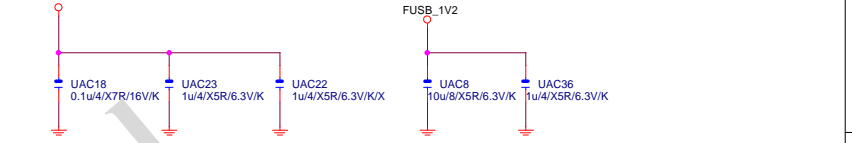
### 3.3V to 1.8V Voltage Regulator

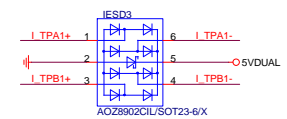
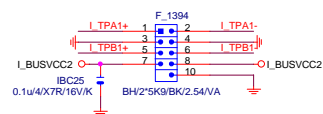
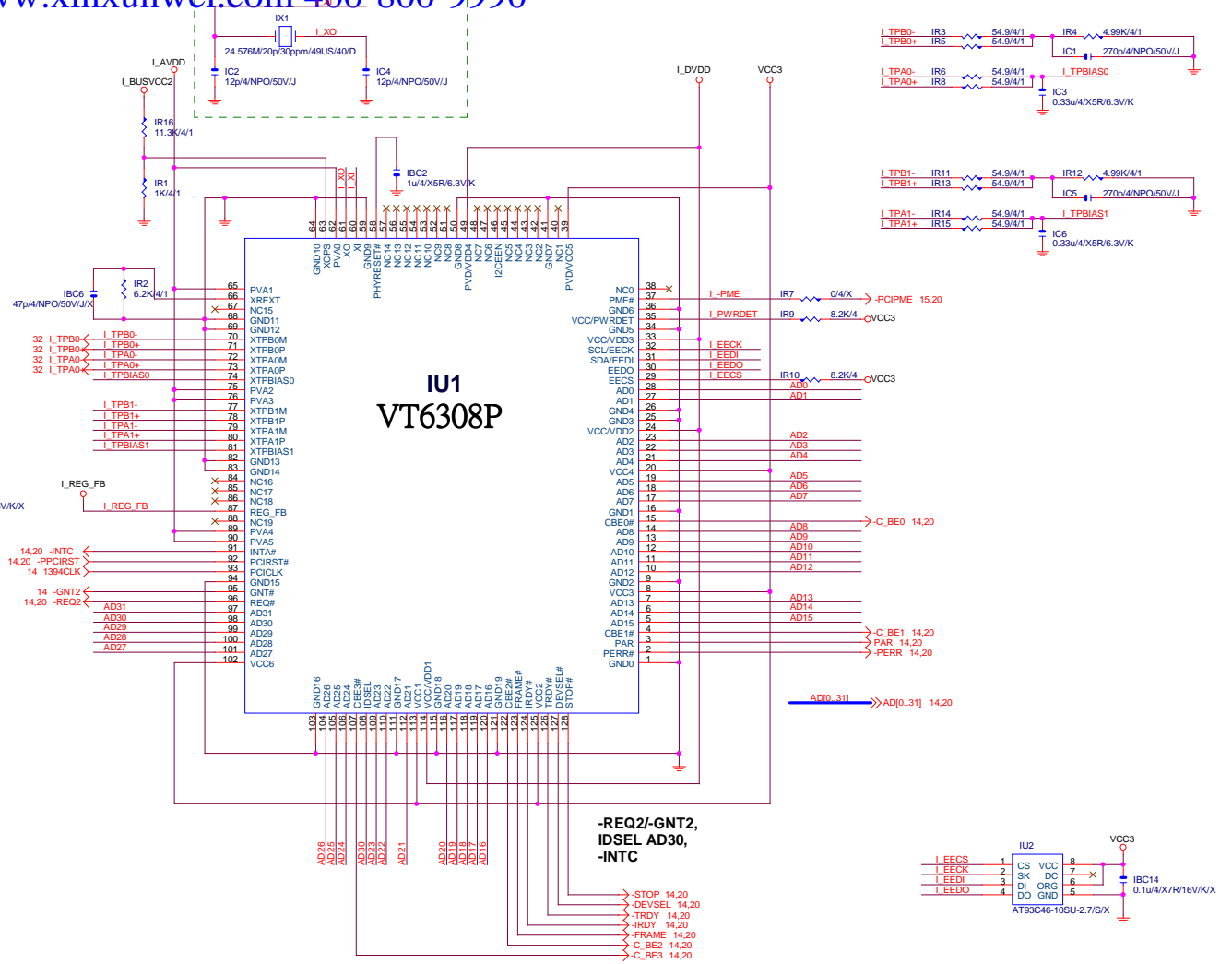
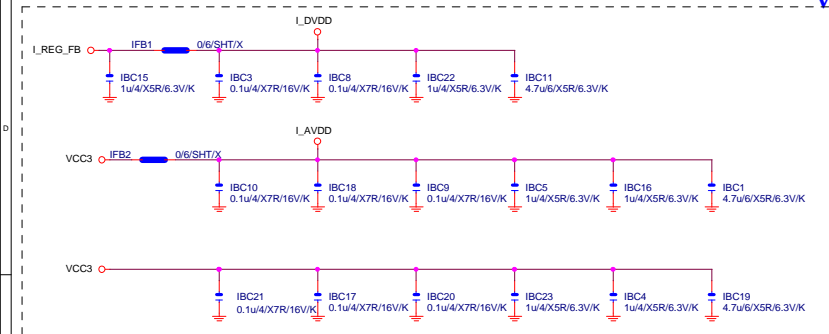


90 歐姆:[20/4.5/7.5/4.5/20]

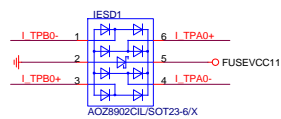




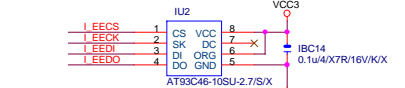




Place close to Header or connector



Place close to Header or connector



Gigabyte Technology			
TI TSB43AB23 1394			
Size	Document Number	Rev	1.11
Custom	GA-990FXA-UD3		
Date	Monday, May 07, 2012	Sheet	35 of 35